2022 Q3 Cadence Taiwan Training Schedule

cadence™

Click the 'Course Name' to the Course Description Page

Course Code (US)	Course Name	Duration (Day)	Jul	Aug	Sep	Location	Fees Per person/Per day (Tax Incl.)
Custom Design with Virtuoso Technology							
ES_84460	Virtuoso Layout Suite L - IC6.1.8 //Virtuoso Layout Design Basics	1	8			Hsinchu	TWD 6,000
ES_84462	Virtuoso Layout Suite XL -IC6.1.7 //Virtuoso Connectivity-Driven Layout Transition	2	21-22			Hsinchu	TWD 12,000
ES_83018	Skill Language Programming -v6.1.8	2		10-11		Hsinchu	TWD 10,400
ES_84453	Skill Programming for IC Layout Design - v6.1.6	1			1	Hsinchu	TWD 5,200
ES_86253-6	ADE Explorer and Assembler v6.1.8 (S1~S4)	2			28-29	Hsinchu	TWD 12,000
ES_84474	Virtuoso Spectre RF - v6.1	2		4-5		Hsinchu	TWD 12,000
ES_82086	Analog Modeling with Verilog -A - Spectre17.1	1	19			Hsinchu	TWD 6,000
ES_84468	Mixed Signal Simulations Using Spectre AMS Designer v20.09	1			14	Hsinchu	TWD 6,000
(Q2&Q4 only) 2022Q4	Assura DRC Verification - v3.1.7	1				Hsinchu	TWD 6,000
	Assura LVS Verification- v3.1.7	1				Hsinchu	TWD 6,000
	Assura DRC/ LVS Rules Writer - v3.1.4	2				Hsinchu	TWD 12,000
ES_84465	Quantus Transistor-Level v 19.1 - T1: Overview and Technology Setup; & T2: Parasitic Extraction	1			8	Hsinchu	TWD 6,000
Digital Design and Signoff							
ES_86141	Innovus Implementation System (Block) v21.1	3		24-25-26		Hsinchu	TWD 18,000
ES_86142	Innovus Implementation System (Hierarchical) v20.1	1			13	Hsinchu	TWD 6,000
ES_82130	Abstract Generator - v5.1.41	1	15			Hsinchu	TWD 6,000
ES_86143	Low-Power Flow with Innovus Implementation System v21.1 (aka: Low Power Workshop-Backend Flow)	1		16		Hsinchu	TWD 6,000
ES_86220	Genus Synthesis Solution with Stylus Common UI v20.1	2	26-27			Hsinchu	TWD 12,000
ES_82169	Voltus Power-Grid Analysis and Signoff v20.1	2			15-16	Hsinchu	TWD 12,000
ES_82147	Tempus Signoff Timing Analysis and Closure v20.1	1			30	Hsinchu	TWD 6,000
Equivalence Checking							
ES_82123	Conformal Equivalence Checking v21.1	1	7			Hsinchu	TWD 6,000
ES_82142	Encounter Conformal Constraint Designer (SDC/CDC Checks)	1	20			Hsinchu	TWD 6,000
ES_82156	Conformal Low-Power Verification v20.1	1			27	Hsinchu	TWD 6,000
ES_82194	Encounter Conformal ECO v20.1	1		31		Hsinchu	TWD 6,000
System Design and Verification (FV)							
ES_86218	Xcelium Simulator V19.03	2	13-14			Hsinchu	TWD 12,000
ES_86225	Xcelium Integrated Coverage V20.09	1		23		Hsinchu	TWD 6,000
ES_82159	SystemVerilog Language for Verification v21.1	2			20-21	Hsinchu	TWD 10,400
PCB and Sigrity							
ES_86090	SiP Layout v17.2	3		17-18-19		Hsinchu	TWD 18,000
(Q1&Q3 only) 2022Q3	Allegro High-Speed Constraint Management v17.2	2	28-29			Hsinchu	TWD 12,000
	Sigrity PowerDC and OptimizePI	2			6-7	Hsinchu	TWD 12,000
	PowerSI + Clarity : Wideband Model Extraction Technology	2			22-23	Hsinchu	TWD 12,000
(Q2&Q4 only) 2022Q4	XtractIM : Allegro Sigrity Package Assessment and Model Extraction	2				Hsinchu	TWD 12,000
	SystemSI – Basic	2				Hsinchu	TWD 12,000
	SystemSI – Advanced	2				Hsinchu	TWD 12,000

2022.6.7 updated

Remark
- **Cadence General Tool training= NTD 6,000** (per day/per person)；**Cadence Language training: NTD 5,200** (per day/per person)
- Cadence Taipei Classroom is not scheduled with training in 2022/Q1. (台北教室設備維護中，本季無課程安排在台北。)