2020 Q4 Cadence Taiwan Training Schedule

cadence™

Click Course Name and go to the Course Description

Course Code (US)	Course Name	Duration (Day)	Oct	Nov	Dec	Location	Fees Per person/Per day (Tax Incl.)
Custom IC, Analog and RF Design							
ES_84460	Virtuoso Layout Suite L - IC6.1.8 //Virtuoso Layout Design Basics	1	13			Hsinchu	TWD 6,000
ES_84462	Virtuoso Layout Suite XL -IC6.1.7 //Virtuoso Connectivity-Driven Layout	2		5-6		Hsinchu	TWD 12,000
ES_83018	Skill Language Programming -v6.1.8	2			3-4	Hsinchu	TWD 10,400
ES_84453	Skill Programming for IC Layout Design - v6.1.6	1			18	Hsinchu	TWD 5,200
ES_82083	Virtuoso Analog Design Environment - v 6.1.8	2	7-8			Hsinchu	TWD 12,000
ES_86253-6	ADE Explorer and Assembler v6.1.8 (S1~S4) *(NEW!)*	2	29-30			Hsinchu	TWD 12,000
ES_84474	Virtuoso Spectre RF - v6.1	2		19-20		Hsinchu	TWD 12,000
ES_82086	Analog Modeling with Verilog -A - Spectre17.1	1		10		Hsinchu	TWD 6,000
ES_84468	Virtuoso AMS Designer - v11.1	1			15	Hsinchu	TWD 6,000
(Q2&Q4 only) 2020Q4	Assura DRC Verification - v3.1.7	1		12		Hsinchu	TWD 6,000
	Assura LVS Verification- v3.1.7	1		13		Hsinchu	TWD 6,000
	Assura DRC/ LVS Rules Writer - v3.1.4	2			16-17	Hsinchu	TWD 12,000
ES_84465	Cadence QRC RF Transistor and Substrate-level Extraction v11.1	1	28			Hsinchu	TWD 6,000
Digital Design and Signoff							
ES_86220	Genus Synthesis Solution with Stylus Common UI v19.1	2		3-4		Hsinchu	TWD 12,000
ES_82160	Innovus Implementation System (Block) v19.1	3	14-15-16			Hsinchu	TWD 18,000
ES_82162	Innovus Implementation System (Hierarchical) v19.1	1		20		Hsinchu	TWD 6,000
ES_82130	Abstract Generator - v5.1.41	1	27			Hsinchu	TWD 6,000
ES_82169	Voltus Power-Grid Analysis and Signoff v18.1	2			1-2	Hsinchu	TWD 12,000
ES_82147	Tempus Signoff Timing Analysis and Closure v18.1	1			9	Hsinchu	TWD 6,000
Equivalence Checking, System Design and Verification							
ES_82123	Conformal Equivalence Checking v19.1	1		11		Hsinchu	TWD 6,000
ES_82142	Encounter Conformal Constraint Designer (SDC/CDC Checks) - v16.2	1	6			Hsinchu	TWD 6,000
ES_82156	Conformal Low-Power Verification v19.1	1			8	Hsinchu	TWD 6,000
ES_82194	Encounter Conformal ECO v19.1	1		24		Hsinchu	TWD 6,000
ES_86218	Xcelium Simulator V19.03	2	20-21			Hsinchu	TWD 12,000
ES_86225	Xcelium Integrated Coverage V17.04	1		17		Hsinchu	TWD 6,000
ES_82159	SystemVerilog Language for Verification v9.2	2			22-23	Hsinchu	TWD 10,400
PCB and Sigrity							
ES_86090	SiP Layout v17.2	3		25-26-27		TPE or HC	TWD 18,000
(Q1&Q3 only)	Allegro High-Speed Constraint Management v17.2	2				TPE or HC	TWD 12,000
	Sigrity PowerDC and OptimizePI	2				TPE or HC	TWD 12,000
	PowerSI + Clarity : Wideband Model Extraction Technology	2				TPE or HC	TWD 12,000
(Q2&Q4 only) 2020Q4	XtractIM : Allegro Sigrity Package Assessment and Model Extraction	2	22-23			TPE or HC	TWD 12,000
	SystemSI – Basic	2		11-12		TPE or HC	TWD 12,000
	SystemSI – Advanced	2			17-18	TPE or HC	TWD 12,000
推廣體驗(Workshop) - 免費 (FREE)							
(Q1&Q3 only)	【Workshop】Universal Verification Methodology (UVM)-System Verilog Workshop	1				Hsinchu	TWD 0
n/a	【Workshop】Low Power Workshop-Frontend Flow	1			10	Hsinchu	TWD 0
n/a	【Workshop】Low Power Workshop-Backend Flow	1			11	Hsinchu	TWD 0

2020.9.3 updated

註： ● 收費標準：**Cadence General Tool training= NTD 6,000** (每人/每天)；**Cadence Language training: NTD 5,200** (每人/每天)

● SPB/Sigrity課程，地點為「TPE or HC」，係指：最後開課地點，取決於學員公司所在地大宗者，辦於Cadence新竹或台北辦公室