cadence

2020 Q3 Cadence Taiwan Training Schedule

按下課程連結，可以看到課程介紹

Course Code (US)		天數	July	Aug	Sept	地點	課程費用/每人次 (含稅)
Custom IC, Analog and RF Design							
ES_84460	Virtuoso Layout Suite L - v6.1.8 //Virtuoso Layout Design Basics	1	7			新竹	TWD 6,000
ES_84462	Virtuoso Layout Suite XL - v6.1.5 //Virtuoso Connectivity-Driven Layout	2	28-29			新竹	TWD 12,000
ES_83018	Skill Language Programming -v6.1.8	2			9-10	新竹	TWD 10,400
ES_84453	Skill Programming for IC Layout Design - v6.1.6	1			24	新竹	TWD 5,200
ES_82083	Virtuoso Analog Design Environment - v 6.1.8	2	14-15			新竹	TWD 12,000
ES_84474	Virtuoso Spectre RF - v6.1	2		13-14		新竹	TWD 12,000
ES_82086	Analog Modeling with Verilog -A - Spectre17.1	1		25		新竹	TWD 6,000
ES_84468	Virtuoso AMS Designer - v11.1	1			15	新竹	TWD 6,000
(二四季排課) 2020Q4	Assura DRC Verification - v3.1.7	1				新竹	TWD 6,000
	Assura LVS Verification- v3.1.7	1				新竹	TWD 6,000
	Assura DRC/ LVS Rules Writer - v3.1.4	2				新竹	TWD 12,000
ES_84465	Cadence QRC RF Transistor and Substrate-level Extraction v11.1	1			17	新竹	TWD 6,000
Digital Design and Signoff							
ES_86220	Genus Synthesis Solution with Stylus Common UI v19.1	2		4-5		新竹	TWD 12,000
ES_82160	Innovus Implementation System (Block) v19.1	3	8-9-10			新竹	TWD 18,000
ES_82162	Innovus Implementation System (Hierarchical) v19.1	1		12		新竹	TWD 6,000
ES_82130	Abstract Generator - v5.1.41	1	17			新竹	TWD 6,000
ES_82169	Voltus Power-Grid Analysis and Signoff v18.1	2			1-2	新竹	TWD 12,000
ES_82147	Tempus Signoff Timing Analysis and Closure v18.1	1			11	新竹	TWD 6,000
Equivalence Checking, System Design and Verification							
ES_82123	Conformal Equivalence Checking v19.1	1		11		新竹	TWD 6,000
ES_82142	Encounter Conformal Constraint Designer (SDC/CDC Checks) - v16.2	1	16			新竹	TWD 6,000
ES_82156	Low-Power Verification with Encounter Conformal- v18.1	1			8	新竹	TWD 6,000
ES_82194	Encounter Conformal ECO v18.1	1		18		新竹	TWD 6,000
ES_86218	Xcelium Simulator V19.03	2	21-22			新竹	TWD 12,000
ES_86225	Xcelium Integrated Coverage V17.04	1		26		新竹	TWD 6,000
ES_82159	SystemVerilog Language for Verification v9.2	2			22-23	新竹	TWD 10,400
PCB and Sigrity							
ES_86090	SiP Layout v17.2	3		19-20-21		台北or新竹	TWD 18,000
(一三季排課)	Allegro High-Speed Constraint Management v17.2	2	23-24			台北or新竹	TWD 12,000
	PowerDC + Static Thermal + OptimizePI : The consideration of PI analysis	2		6-7		台北or新竹	TWD 12,000
	PowerSI + Clarity : Wideband Model Extraction Technology	2			29-30	台北or新竹	TWD 12,000
(二四季排課) 2020Q4	XtractIM : Allegro Sigrity Package Assessment and Model Extraction	2				台北or新竹	TWD 12,000
	SystemSI – Basic	2				台北or新竹	TWD 12,000
	SystemSI – Advanced	2				台北or新竹	TWD 12,000
推廣體驗(Workshop) - 免費 (FREE)							
(一三季排課)	【Workshop】Universal Verification Methodology (UVM)-System Verilog Workshop	1	30			新竹	TWD 0
n/a	【Workshop】Low Power Workshop-Frontend Flow	1			3	新竹	TWD 0
n/a	【Workshop】Low Power Workshop-Backend Flow	1			4	新竹	TWD 0

2020.2.27 updated

註：
- 收費標準：**Cadence General Tool training= NTD 6,000** (每人/每天)；**Cadence Language training: NTD 5,200** (每人/每天)
- SPB/Sigrity課程，地點為「台北or新竹」，係指：最後開課地點，取決於學員公司所在地大宗者，辦於Cadence新竹或台北辦公室