2019 Q2 Cadence Training Schedule

cadence™

按下課程連結，可以看到課程介紹

Course Code (US)		天數	4月	5月	6月	地點	課程費用/每人次 (含稅)
CIC							
ES_84460	Virtuoso Layout Suite L - v6.1.7 //Virtuoso Layout Design Basics	1	9			新竹	TWD 6,000
ES_84462	Virtuoso Layout Suite XL - v6.1.5 //Virtuoso Connectivity-Driven Layout	2	23-24			新竹	TWD 12,000
ES_83018	Skill Language Programming -v6.1.7	2		16-17		新竹	TWD 10,400
ES_84453	Skill Programming for IC Layout Design - v6.1.6	1			11	新竹	TWD 5,200
ES_82083	Virtuoso Analog Design Environment - v 6.1.7	2	11-12			新竹	TWD 12,000
ES_84474	Virtuoso Spectre RF - v6.1	2		8-9		新竹	TWD 12,000
ES_82086	Analog Modeling with Verilog -A - v13.1	1		21		新竹	TWD 6,000
ES_84468	Virtuoso AMS Designer - v11.1	1			26	新竹	TWD 6,000
(二四季排課) 2019Q2	Assura DRC Verification - v3.1.7 (雙季排課)	1	25			新竹	TWD 6,000
	Assura LVS Verification- v3.1.7 (雙季排課)	1	26			新竹	TWD 6,000
	Assura DRC/ LVS Rules Writer - v3.1.4 (雙季排課)	2		23-24		新竹	TWD 12,000
ES_84465	Cadence QRC RF Transistor and Substrate-level Extraction v11.1	1		10		新竹	TWD 6,000
ICD							
ES_86164	Genus Synthesis Solution v16.1	2		28-29		新竹	TWD 12,000
ES_82160	Innovus Implementation System (Block) v18.1	3	17-18-19			新竹	TWD 18,000
ES_82162	Innovus Implementation System (Hierarchical) v18.1	1		30		新竹	TWD 6,000
ES_82130	Abstract Generator - v5.1.41	1	16			新竹	TWD 6,000
ES_82169	Voltus Power-Grid Analysis and Signoff v17.1	2			18-19	新竹	TWD 12,000
ES_82147	Tempus Signoff Timing Analysis and Closure v17.2	1			12	新竹	TWD 6,000
FED/AVS							
ES_82123	Logic Equivalence Checking with Conformal EC- v17.1	1	10			新竹	TWD 6,000
ES_82142	Encounter Conformal Constraint Designer (SDC/CDC Checks) - v16.2	1		7		新竹	TWD 6,000
ES_82156	Low-Power Verification with Encounter Conformal- v18.1	1			25	新竹	TWD 6,000
ES_82194	Encounter Conformal ECO v15.1	1		22		新竹	TWD 6,000
ES_86218	Xcelium Simulator V17.04	2			20-21	新竹	TWD 12,000
ES_86225	Xcelium Integrated Coverage V17.04	1	30			新竹	TWD 6,000
ES_82159	SystemVerilog Language for Verification v9.2	2		14-15		新竹	TWD 10,400
SPB/Sigrity							
ES_86081	SiP Layout v17.2	3	10-11-12			台北or新竹	TWD 18,000
(一三季排課)	Allegro High-Speed Constraint Management v17.2 (雙季排課)	2				台北or新竹	TWD 12,000
	PowerDC + Static Thermal + OptimizePI : The Consideration of PI Analysis (雙季排課)	2				台北or新竹	TWD 12,000
	PowerSI + 3DEM : Wideband Model Extraction Technology (雙季排課)	2				台北or新竹	TWD 12,000
(二四季排課) 2019Q2	XtractIM : Allegro Sigrity Package Assessment and Model Extraction (雙季排課)	2			12-13	台北or新竹	TWD 12,000
	SystemSI – Basic (雙季排課)	2		22-23		台北or新竹	TWD 12,000
	SystemSI – Advacne (雙季排課)	2		29-30		台北or新竹	TWD 12,000
推廣體驗(Workshop) - 免費							
(一三季排課)	【Workshop】Universal Verification Methodology (UVM)-System Verilog Workshop (雙季排課)	1				新竹	TWD 0
n/a	【Workshop】Low Power Workshop-Frontend Flow	1			27	新竹	TWD 0
n/a	【Workshop】Low Power Workshop-Backend Flow	1			28	新竹	TWD 0

註：

2019.03.04 updated

- 收費標準：**Cadence General Tool training= NTD 6,000** (每人/每天)；**Cadence Language training: NTD 5,200** (每人/每天)
- SPB/Sigrity課程，地點為「台北or新竹」，係指：最後開課地點，取決於學員公司所在地大宗者，辦於Cadence新竹或台北辦公室