

# CADENCE KOREA ES SCHEDULE - 1st half of 2018

11/23/2017

Course Name	Instructor	Course ID	Length	S_Date	E_Date	Location
<b>Custom IC Design</b>						
Virtuoso Analog simulation Technique	SWSEO	NA	2	1/18/2018	1/19/2018	IDEC (대전Kaist)
SKILL Language Programming	HSHAN/KHOH/SYLEE	83018	3	2/7/2018	2/9/2018	Cadence Korea
Virtuoso Layout Pro(Virtuoso_XL & GXL): T3 , T4 , T5	TJLEE	85092	2	2/22/2018	2/23/2018	Cadence Korea
Mixed Signal Simulation Using AMS Designer	SCLEE	NA	2	2/8/2018	2/9/2018	IDEC (대전Kaist)
Spectre Simulator Fundamentals vMMSIM 15.1 (S1,S2,S3,S4)	SCLEE	86210	2	3/8/2018	3/9/2018	Cadence Korea
Virtuoso Layout Design Basics vIC 6.1.6 & Virtuoso Layout Pro: T2	SECHOI	86131	2	3/19/2018	3/20/2018	Cadence Korea
Mixed Signal Simulation Using AMS Designer	SCLEE	86135	2	3/29/2018	3/30/2018	Cadence Korea
Virtuoso Analog Design Environment	SCLEE	82083	2	4/19/2018	4/20/2018	Cadence Korea
Virtuoso Analog Simulation : ADE (G)XL (T1, T2, T3, T4)	SCLEE	86209	2	6/4/2018	6/5/2018	Cadence Korea
SKILL Language Programming	HSHAN/KHOH/SYLEE	83018	3	6/20/2018	6/22/2018	Cadence Korea
<b>Digital IC Design</b>						
Innovus Implementation System (Block) v17.1	KSPARK	86141	3	2/19/2018	2/21/2018	Cadence Korea
Tempus Signoff Timing Analysis and Closure	JKKIM	82147	2	2/26/2018	2/27/2018	Cadence Korea
Genus Synthesis Solution v16.1	JYCHOI / JHCHOI	86164	2	3/6/2018	3/7/2018	Cadence Korea
Innovus Implementation System (Block)	HJKIM	NA	2	3/15/2018	3/16/2018	IDEC (대전Kaist)
Conformal Equivalence Check & Conformal ECO	DRSUH	86133	3	3/14/2018	3/16/2018	Cadence Korea
Innovus Implementation System (Hierarchical) v17.1	HSYOON	86142	3	3/21/2018	3/23/2018	Cadence Korea
SystemC Synthesis with Stratus HLS	JCKIM	86170	3	4/11/2018	4/13/2018	Cadence Korea
Innovus Implementation System (Block) v17.1	HJBAE	86141	3	5/16/2018	5/18/2018	Cadence Korea
Conformal Low Power & IEEE1801	KPARK	86125	3	5/23/2018	5/25/2018	Cadence Korea
<b>Functional Verification</b>						
Incisive SystemC, VHDL, and Verilog Simulation	IHJUNG	82115	2	2/12/2018	2/13/2018	Cadence Korea
SystemC Synthesis with Stratus HLS	JCKIM	86170	3	4/11/2018	4/13/2018	Cadence Korea
Incisive Comprehensive Coverage with IMC	IHJUNG	82136	2	4/17/2018	4/18/2018	Cadence Korea
Acceleration and Emulation Using Palladium XP	ICJANG	84503	1	4/27/2018	4/27/2018	Cadence Korea
Incisive SystemC, VHDL, and Verilog Simulation	IHJUNG	82115	2	6/14/2018	6/15/2018	Cadence Korea
<b>Silicon-Package-Board Co-Design</b>						
Allegro PCB Librarian	KHLEE	86022	1	1/15/2018	1/15/2018	Cadence Korea
Allegro Design Entry HDL Front-to-Back Flow	KHLEE	86015	2	1/16/2018	1/17/2018	Cadence Korea
Allegro PCB Editor Basic Techniques	KHLEE	86097	3	1/24/2018	1/26/2018	Cadence Korea
Allegro Sigrity SI Foundations	MYHAN	85073	2	2/5/2018	2/6/2018	Cadence Korea
Sigrity PowerSI for Model Generation and Analysis	JHLEE	86137	1	2/26/2018	2/26/2018	Cadence Korea
Allegro Sigrity Power-Aware Parallel Bus Analysis	DHKANG	85060	1	2/27/2018	2/27/2018	Cadence Korea
Allegro Sigrity System Serial Link Analysis	HJLEE	85061	1	3/2/2018	3/2/2018	Cadence Korea
Sigrity PowerDC and OptimizePI	JHLEE	85084	1	3/5/2018	3/5/2018	Cadence Korea
Allegro Sigrity PI	MYHAN	86060	1	3/6/2018	3/6/2018	Cadence Korea
SiP Layout	KHLEE	86090	3	3/21/2018	3/23/2018	Cadence Korea
Allegro PCB Librarian	JOYLEE	86022	1	4/4/2018	4/4/2018	Cadence Korea
Allegro Design Entry HDL Front-to-Back Flow	JOYLEE	86015	2	4/5/2018	4/6/2018	Cadence Korea
Allegro PCB Editor Basic Techniques	JOYLEE	86097	3	4/23/2018	4/25/2018	Cadence Korea
Allegro Sigrity SI Foundations	MYHAN	85073	2	5/2/2018	5/3/2018	Cadence Korea
Sigrity PowerSI for Model Generation and Analysis	JHLEE	86137	1	5/4/2018	5/4/2018	Cadence Korea
Allegro Sigrity Power-Aware Parallel Bus Analysis	DHKANG	85060	1	5/14/2018	5/14/2018	Cadence Korea
Allegro Sigrity System Serial Link Analysis	HJLEE	85061	1	5/15/2018	5/15/2018	Cadence Korea
Allegro Sigrity PI	MYHAN	86060	1	6/18/2018	6/18/2018	Cadence Korea
Sigrity PowerDC and OptimizePI	JHLEE	85084	1	6/19/2018	6/19/2018	Cadence Korea
SiP Layout	JOYLEE	86090	3	6/25/2018	6/27/2018	Cadence Korea
Allegro PCB Editor SKILL Programming Language	MYHAN	86099	3	6/27/2018	6/29/2018	Cadence Korea

\* 해당교육의 강사는 변경 될 수도 있습니다.

1. 교육신청

[https://www.cadence.com/content/cadence-www/global/ko\\_KR/home/training/all-courses.html](https://www.cadence.com/content/cadence-www/global/ko_KR/home/training/all-courses.html)

\* 상기 일정은 내부사정으로 인해 변경될 수도 있습니다.

2. 교육문의

Email: [training\\_korea@cadence.com](mailto:training_korea@cadence.com) / Tel: 031-728-3036

\* IDEC 교육은 해당기관 주관으로 진행되는 외부교육입니다.  
-장소: IDEC (대전 Kaist)

3. 교육마감

교육시작 3일전 ( Working day 기준 )