Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
## IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Tier</th>
<th>Days</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## SI/PI Analysis

<table>
<thead>
<tr>
<th>Course</th>
<th>Tier</th>
<th>Days</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allegro Sigrity™ SI Foundations</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro Sigrity PI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sigrity PowerDC™ and OptimizePI™</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clarity 3D Field Solver</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

© 2019 Cadence Design Systems, Inc.
Digital Design and Signoff Learning Map

**Synthesis and Test**
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Flow with Genus Synthesis Solution
- Test Synthesis Using Genus Synthesis Solution
- Advanced Synthesis with Genus Stylus Common UI
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

**Implementation**
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO

Cadence® RTL-to-GDSII Flow

New Course
Number of days for instructor-led course
Online Course Available
Digital Badge Available

© 2019 Cadence Design Systems, Inc.
Tensilica Processor IP Learning Map

Tensilica® Xtensa® NX Processor Fundamentals

Tensilica® Xtensa® NX Processor Interfaces

Tensilica® Xtensa® NX Hardware Verification and EDA

Tensilica Instruction Extension Language and Design

Tensilica System Modeling using XTSC

ConnX DSP

Tensilica ConnX B10 DSP

Tensilica ConnX B20 DSP

Tensilica Vision Q7 DSP

Vision DSP

© 2019 Cadence Design Systems, Inc.