Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- Allegro Design Entry HDL Front-to-Back Flow
- Allegro Design Entry Using OrCAD® Capture
- OrCAD CIS
- OrCAD Capture Constraint Manager PCB Flow
- Allegro EDM Design Entry HDL Front-to-Back Flow
- Allegro Team Design Authoring
- Analog Simulation with PSpice®

## PCB Design
- Allegro PCB Editor Basic Techniques
- Allegro PCB Editor Intermediate Techniques
- Allegro PCB Router Basics
- Allegro PCB Editor Advanced Methodologies
- Allegro High-Speed Constraint Management
- Allegro Update Training
- Advanced Design Verification with the RAVEL Programming Language

## SI/PI Analysis
- Essential High-Speed PCB Design for Signal Integrity
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
- Allegro Sigri™ SI Foundations
- Allegro Sigry PI
- Sigri PowerDC™ and OptimiPI™
- Sigri Aurora
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM
- Clarity 3D Solver
- Celsius Thermal Solver

## Library Development
- Allegro PCB Librarian
- Allegro EDM PCB Librarian
- Allegro Design Entry HDL SKILL® Programming Language
- Allegro PCB Editor SKILL Programming Language
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- New Course
- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available

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Custom IC, Analog and RF Design Learning Map

Circuit Design, Simulation, Modeling and RF Design

Analog Modeling with Verilog-A
- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model
- Behavioral Modeling with Verilog AMS
- Behavioral Modeling with VHDL-AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

Virtuoso Schematic Editor
- Virtuoso Visualization and Analysis

Virtuoso® ADE Explorer & Assembler Series
- S1 ADE Explorer & Single Test Corner Analysis
- S2 ADE Assembler & Multi Test Corner Analysis
- S3 Sweeping Variables and Simulating Corners
- S4 Monte Carlo, Real-Time Tuning & Run Plans

Design Checks and Asserts

Virtuoso® ADE Verifier Series
- S1 Setup, Run, & View Verifier Results
- S2 Reference Flow and Analog Coverage Using the Setup Library Assistant

5G mmWave Handset System Design – S1 RFIC (Transceiver) Design

Spectre® Simulator Fundamentals Series
- S1 Spectre Basics
- S2 Large-Signal
- S3 Small-Signal
- S4 Spectre MDL

Spectre Accelerated Parallel Simulator (APS)

Spectre XPS for Mixed-Signal Designs

Virtuoso® Spectre® Pro Series
- S1 DC Algorithm
- S2 AC, XF, STB, Noise
- S3 Transient Algorithm
- S4 Fourier Transform
- S5 Transient Noise

Spectre® RF Shooting Newton

Spectre® RF Harmonic Balance

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Digital Design and Signoff Learning Map

Synthesis and Test
- Design For Test Fundamentals
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Stylus Common UI
  - Test Synthesis with Genus Stylus Common UI
  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

Virtuoso® Digital Implementation
- Virtuoso® Digital Implementation
  - Innovus™ Implementation System (Block)
  - Innovus Implementation System (Hierarchical)
  - Low-Power Flow with Innovus Implementation System

Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure

Voltus™ Power-Grid Analysis and Signoff

Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal Low-Power Verification Using IEEE1801
- Conformal ECO

Cadence® RTL-to-GDSII Flow

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System Design and Verification Learning Map

Design and Verification Languages

- **Verilog Language and Application**
- **SystemVerilog for Design and Verification**
- **SystemVerilog Assertions**
- **SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification**
- **Perl for EDA Engineering**
- **Tcl Scripting for EDA**
- **VHDL Language and Application**
- **C++ Language Fundamentals for Design and Verification**
- **SystemC® Language Fundamentals**
- **SystemC Synthesis with Stratus HLS**
- **SystemC Transaction-Level Modeling TLM 2.0**
- **JasperGold® Formal Fundamentals**
- **SVA, Formal & JasperGold® Fundamentals for Designers**
- **JasperGold® Formal Expert**

- **Real Modeling with Verilog AMS**
- **Real Modeling with SystemVerilog**
- **SystemVerilog Accelerated Verification Using UVM**
- **SystemVerilog Advanced Register Verification Using UVM**
- **Essential SystemVerilog for UVM (optional)**

- **Digital Badge Available**
- **New Course**
- **Number of days for instructor-led course**
- **Tiers of Cadence products used in course**
- **Online Course Available**

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