Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents
- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- **Beginner**
  - Allegro® Design Entry HDL Front-to-Back Flow
  - Allegro Design Entry HDL Basics
  - Allegro System Capture
  - Allegro Design Reuse
  - Allegro AMS Simulator

## PCB Design
- **Advanced**
  - Allegro PCB Editor Basic Techniques
  - OrCAD Capture
  - OrCAD Capture Constraint Manager PCB Flow
  - Allegro EDM Design Entry HDL Front-to-Back Flow
  - Allegro Team Design Authoring
  - Analog Simulation with PSpice®
  - Allegro PCB Editor Intermediate Techniques
  - Allegro PCB Editor Advanced Methodologies
  - Allegro PCB Router Basics
  - Allegro High-Speed Constraint Management
  - Allegro Update Training
  - Advanced Design Verification with the RAVEL Programming Language

## SI/PI Analysis
- **Beginner**
  - Essential High-Speed PCB Design for Signal Integrity
  - PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
  - Allegro Sigrity™ SI Foundations
  - Allegro Sigrity PI
  - Sigrity PowerDC™ and OptimizePI™
  - Sigrity Aurora
  - TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
  - Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM
  - Clarity 3D Solver
  - Celsius Thermal Solver

## Library Development
- **Beginner**
  - Allegro PCB Librarian
  - Allegro EDM PCB Librarian
  - Allegro Design Entry HDL SKILL® Programming Language
  - Allegro PCB Editor SKILL Programming Language

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**New Course**

**Number of days for instructor-led course**

**Tiers of Cadence products used in course**

**Online Course Available**

**Digital Badge Available**

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## IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Tiers</th>
<th>Number of days for instructor-led course</th>
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<tr>
<td>SiP Layout</td>
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<tr>
<td>Allegro® Package Designer</td>
<td>4</td>
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<tr>
<td>Allegro FPGA System Planner</td>
<td>2</td>
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<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
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<td>OrbitIO™ System Planner</td>
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<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
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<td>Allegro Package Designer Plus</td>
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## SI/PI Analysis

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<tr>
<td>Allegro Sigrity™ SI Foundations</td>
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<tr>
<td>Allegro Sigrity PI</td>
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<td>TopXplorer SystemSI for Parallel Bus and Serial Link Analysis</td>
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<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
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<td>Clarity 3D Solver</td>
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<td>Celsius Thermal Solver</td>
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</tbody>
</table>

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Digital Design and Signoff Learning Map

Synthesis and Test
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Stylus Common UI
  - Test Synthesis with Genus Stylus Common UI
  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

Implementation
- Innovus™ Implementation System (Block)
  - Innovus Implementation System (Hierarchical)
  - Low-Power Flow with Innovus Implementation System
  - Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

Silicon Signoff
- Basic Static Timing Analysis
  - Tempus™ Signoff Timing Analysis and Closure
  - Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking
- Conformal® Equivalence Checking
  - Conformal Low-Power Verification
  - Conformal ECO

Cadence® RTL-to-GDSII Flow
Simulation, Coverage and Debug

- Xcelium™ Simulator
  - 2

- Foundations of Metric-Driven Verification
  - 1

- Xcelium Integrated Coverage
  - 2

- Low-Power Simulation with CPF
  - 2

- Low-Power Simulation with IEEE1801 UPF
  - 2

- VIP Basic Building Blocks and Usage
  - 2

- Metrics-Driven Verification Using vManager™
  - 2

- vManager Tool Usage in Batch Mode
  - 0.5

- Perspec™ System Verifier - Basic
  - 5

- Incisive Functional Safety Simulator
  - 1

- Specman® Fundamentals for Block-Level Environment Developers
  - 5

- Specman Advanced Verification
  - 4

New Course - Number of days for instructor-led course - Tiers of Cadence products used in course - Online Course Available - Digital Badge Available

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System Design and Verification Learning Map

Design and Verification Languages

Verilog Language and Application

SystemVerilog for Design and Verification

UVM

SystemVerilog Accelerated Verification Using UVM

SystemVerilog Advanced Register Verification Using UVM

SystemVerilog Assertions

JasperGold® Formal Fundamentals

JasperGold® Formal Expert

VHDL Language and Application

C++ Language Fundamentals for Design and Verification

SystemC® Language Fundamentals

SystemC Synthesis with Stratus HLS

SystemC Transaction-Level Modeling TLM2.0

SystemVerilog for Design and Verification

Real Modeling with Verilog AMS

Real Modeling with SystemVerilog

SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

Perl for EDA Engineering

Tcl Scripting for EDA

New Course

Number of days for instructor-led course

Tiers of Cadence products used in course

Online Course Available

Digital Badge Available

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