Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents
- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

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### Logic Design
- **Beginner**
  - Allegro® Design Entry HDL Front-to-Back Flow 3 days
  - Allegro Design Entry HDL Basics 1 day
  - Allegro System Design Authoring 1 day
  - Allegro Design Reuse 1 day
  - Allegro AMS Simulator Advanced Analysis 1 day

### PCB Design
- **Beginner**
  - Allegro Design Entry Using OrCAD® Capture 2 days
  - OrCAD CIS 1 day
  - Allegro System Architect 2 days
  - Allegro Design Workbench for Engineers and Designers 1 day
  - Allegro AMS Simulator Advanced Analysis 1 day

### SI/PI Analysis
- **Beginner**
  - Allegro PCB Editor Basic Techniques 3 days
  - Allegro PCB Editor Intermediate Techniques 2 days
  - Allegro PCB Router Basics 2 days
  - Allegro PCB Editor Advanced Methodologies 1 day
  - Allegro High-Speed Constraint Management 1 day
  - Allegro Update Training 1 day
  - Advanced Design Verification with the RAVEL Programming Language 1 day
  - Essential High-Speed PCB Design for Signal Integrity 3 days
  - PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials 2 days
  - Allegro Sigrity™ SI Foundations 2 days
  - Allegro Sigrity PI 2 days
  - Sigriy PowerDC™ and OptimizePI™ 1 day
  - Sigriy SystemSI™ for Parallel Bus and Serial Link Analysis 1 day
  - Sigriy PowerSI® for Model Generation and Analysis 2 days

### Library Development
- **Beginner**
  - Allegro PCB Librarian 2 days
  - Allegro Design Workbench for Librarians 2 days
  - Allegro Design Workbench for Administrators 2 days
  - Allegro PCB Editor SKILL® Programming Language 3 days
  - Allegro Tool Setup and Configuration 2 days

**New Course**

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| Allegro Sigrity Package Assessment and Model Extraction | Sigtry SystemSI™ for Parallel Bus and Serial Link Analysis  

New Course: Number of days for instructor-led course  
L: Low  
M: Medium  
H: High  
Tiers of Cadence products used in course  
Online Course Available  
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## Custom IC, Analog and RF Design Learning Map

### IC CAD

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### Layout Design and Advanced Nodes

#### Virtuoso® Layout Design Basics
- T1: Env. and Basic Commands
- T2: Create and Edit Commands
- T3: Basic Commands
- T4: Advanced Commands
- T5: Interactive Routing
- T6: Constraint-Driven Flow and Power Routing
- T7: Module Generator and Floorplanner
- T8: Debugging Layout Issues

#### Virtuoso® Connectivity-Driven Layout Transition
- Virtuoso Abstract Generator
- Virtuoso Floorplanner
- Virtuoso Space-Based Router

#### Virtuoso® Advanced-Node Series – ICADV
- T1: Place and Route
- T2: Electromigration

### Layout Verification

#### Physical Verification System (PVS)
- T1: Overview and Technology Setup
- T2: Parasitic Extraction
- T3: Extracted View Flows and Advanced Features

#### Assura® Verification DRC/LVS
- T2: Rules-Writer

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