Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

PCB Design and Analysis Learning Map

Beginner ↓ Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow — 3 days, Online
- Allegro Design Entry HDL Basics — 1 day, Online
- Allegro System Design Authoring — NEW — 1 day, Online
- Allegro System Architect — 2 days, Online
- Allegro Design Reuse — 1 day, Online
- Allegro AMS Simulator — 3 days
  - Allegro AMS Simulator Advanced Analysis — 1 day, Online
- Allegro Design Entry Using OrCAD® Capture — 2 days, Online
- OrCAD CIS — 1 day
- Allegro Team Design Authoring — 1 day, Online
- Allegro Design Workbench for Engineers and Designers — 1 day, Online
- Analog Simulation with PSpice® — 3 days, Online
  - Analog Simulation with PSpice Advanced Analysis — 1 day, Online

PCB Design

- Allegro PCB Editor Basic Techniques — 3 days, Online
  - Allegro PCB Editor Intermediate Techniques — 2 days, Online
  - Allegro PCB Router Basics — 2 days, Online
  - Allegro PCB Editor Advanced Methodologies — NEW — 1 day, Online
- Allegro High-Speed Constraint Management — 2 days, Online
- Allegro Update Training — NEW — 1 day, Online
- Advanced Design Verification with the RAVEL Programming Language — NEW — 2 days, Online

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity — 3 days
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials — 2 days
- Allegro Sigrity™ SI Foundations — 2 days, Online
- Allegro Sigrity PI — 1 day, Online
- Sigrity PowerDC™ and OptimizePI™ — 1 day, Online
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis — NEW — 3 days, Online
- Sigrity PowerSI® for Model Generation and Analysis — 2 days, Online

Library Development

- Allegro PCB Librarian — 2 days, Online
- Allegro Design Workbench for Librarians — 2 days
- Allegro Design Workbench for Administrators — 2 days
- Allegro Design Entry HDL SKILL® Programming — 3 days, Online
- Allegro PCB Editor SKILL Programming Language — 3 days, Online
- Allegro Tool Setup and Configuration — 2 days, Online

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout — 5 days
- Allegro® Package Designer — 4 days
- Allegro FPGA System Planner — 2 days
- Allegro Sigrity Package Assessment and Model Extraction — 1 day
- OrbitIO™ System Planner — 1 day
- Advanced Design Verification with the RAVEL Programming Language NEW — 2 days

SI/PI Analysis

- Allegro Sigrity™ SI Foundations — 2 days
- Allegro Sigrity PI — 1 day
- Sigrity PowerDC™ and OptimizePI™ — 1 day
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis NEW — 3 days
- Sigrity PowerSI® for Model Generation and Analysis — 2 days

Beginner

Advanced

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

Virtuoso® Analog Design Environment

L 3

Virtuoso Analog Simulation Series NEW

- **T1**: Introduction to the Virtuoso ADE XL Environment — XL 1
- **T2**: Creating Sweeps and Running Corners — XL 0.5
- **T3**: Monte Carlo Simulation Using ADE XL — XL 0.5
- **T4:** Sensitivity Analysis and Circuit Optimization Using ADE GXL — GXL 0.5

Mixed-Signal Simulations Using AMS Designer

3

Analog Modeling with Verilog-A

3

- Behavioral Modeling with / Verilog-AMS / VHDL-AMS — 2
- Real Modeling with / SystemVerilog / Verilog-AMS NEW — 2
- Transistor-Level Power Signoff with Voltus™-Fi NEW — 1.5

Virtuoso Schematic Editor

L XL 2

Virtuoso® ADE Explorer Series NEW

- **S1**: Set Up and Run Analog Simulations Using the Spectre® Simulator — 0.5
- **S2**: Analyzing Simulations Using ViVA XL — 0.5
- **S3**: Corner Analysis and Monte Carlo Simulation — 0.5
- **S4**: Real-Time Tuning, Checks/Asserts, and Reliability Analysis — 0.5

Virtuoso ADE Assembler Series NEW

- **S1:** Introducing the Assembler Environment — 0.5
- **S2**: Sweeping Variables, Simulating Corners and Creating Run Plans — 0.5
- **S3**: Circuit Checks, Device Asserts and Reliability Analysis — 0.5

Virtuoso ADE Verifier NEW

1

Variation Analysis Using the Virtuoso Variation Option NEW

1

Spectre Simulator Fundamentals Series NEW

- **S1**: Spectre Basics — 0.5
- **S2**: Large-Signal — 0.5
- **S3**: Small-Signal — 0.5
- **S4:** Spectre MDL — 0.5

High-Performance Sim. using Spectre Simulators

2

Spectre Accelerated Parallel Simulator (APS) NEW

1

Spectre XPS for Mixed-Signal Designs NEW

1

Virtuoso EAD with LDE

1

Virtuoso Spectre Pro Series

- **S1**: DC Algorithm — 0.5
- **S2**: AC, XF, STB, Noise — 0.5
- **S3**: Transient Algorithm — 0.5
- **S4**: Fourier Transform — 0.5
- **S5**: Transient Noise — 1

Spectre® RF/ Shooting Newton / Harmonic Balance

2

Library Characterization

Cadence® Library Characterization and Validation

2

- Virtuoso Liberate™ MX for Memory Characterization — 2.5
- Cadence Variety™ Statistical Library Characterization — 1

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Custom IC, Analog and RF Design Learning Map

2 of 2 – see prior page

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2 — Online
- SKILL Language Programming Fundamentals — 3
- SKILL Language Programming — 5 — Online
- SKILL Development of Parameterized Cells — 2 — Online
- SKILL Programming for IC Layout Design — 2
- Advanced SKILL Language Programming — 3 — Online

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics — L — 1 — Online
- Virtuoso Connectivity-Driven Layout Transition — L — XL — 2 — Online
  - Virtuoso Abstract Generator NEW — GXL — 1 — Online
  - Virtuoso Floorplanner — GXL — 1 — Online
  - Virtuoso Space-Based Router — GXL — 2 — Online
    - Virtuoso Space-Based Router Express NEW — GXL — 0.5 — Online

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — L — 0.5 — Online
- T2: Create and Edit Commands — L — 0.5 — Online
- T3: Basic Commands — XL — 0.5 — Online
- T4: Advanced Commands — XL — 0.5 — Online
- T5: Interactive Routing — XL — 0.5 — Online
  - T6: Constraint-Driven Flow and Power Routing — XL — GXL — 0.5 — Online
  - T7: Module Generator and Floorplanner — XL — GXL — 0.5 — Online
- T8: Debugging Layout Issues — L — XL — 0.5 — Online

Virtuoso® Advanced-Node Series – ICADV

- Virtuoso Layout for Advanced Nodes — 2 — Online
  - T1: Place and Route NEW — 1 — Online
  - T2: Electromigration NEW — 0.5 — Online

Layout Verification

- Physical Verification System (PVS) — 2 — Online
  - Physical Verification Language Rules-Writer — 2

Quantus™ QRC Transistor-Level Series NEW

- T1: Overview and Technology Setup — 0.5 — Online
  - T2: Parasitic Extraction — 1 — Online
  - T3: Extracted View Flows and Advanced Features — 0.5 — Online

- Assura® Verification DRC/LVS — 3
  - Assura Rules-Writer — 4

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis

- Genus™ Synthesis Solution — 2
- Low-Power Synthesis Flow with Genus Synthesis Solution — 1
- Test Synthesis Using Genus Synthesis Solution — 2
- Advanced Synthesis with Genus Synthesis Solution — 1
- Fundamentals of IEEE 1801 Low-Power Specification Flow — 1
- Modus DFT Software Solution — 1
- Joules™ Power Calculator — 1

Implementation

- Virtuoso® Digital Implementation — 2
- Innovus™ Implementation System — 3
- Innovus Implementation System (Hierarchical) — 1
- Low-Power Flow with Innovus Implementation System — 1
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis — 1
- Analog-on-Top Mixed-Signal Implementation — 2

Silicon Signoff

- Basic Static Timing Analysis — 2
- Tempus™ Signoff Timing Analysis and Closure — 2
- Voltus™ Power-Grid Analysis and Signoff — 2

Equivalence Checking

- Logic Equivalence Checking with Conformal® EC — 2
- Conformal Low-Power Verification — 1
- Conformal ECO — 1
- Conformal Constraint Designer — 1

Cadence® RTL-to-GDS Flow — 2

NEW New Course

Number of days for instructor-led course

Online Course Available

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Acceleration, Emulation, Coverage and Debug

- Incisive® SystemC®, VHDL, and Verilog Simulation — 2
- Incisive Comprehensive Coverage with IMC — 2
- Incisive Simulation Performance Optimization NEW
- Perspec™ System Verifier
- Indago™ Analyzer App (15.2)
- Low-Power Simulation with CPF — 2
- Low-Power Simulation with IEEE1801 UPF — 2
- Incisive Functional Safety Simulator NEW — 1
- The Xcelium™ Simulator NEW — 2
- Cadence® RTL-To-GDSII Flow NEW — 2
- Foundations of Metric-Driven Verification — 1
- Xcelium Integrated Coverage NEW — 2
- Indago Analyzer App (17.10) NEW
- Metric-Driven Verification Using vManager™ NEW — 3
- vManager Tool Usage in Batch Mode — 0.5
- Specman® Fundamentals for Block-level Environment Developers — 5
  - Specman Advanced Verification — 4
- In-Circuit Emulation with Palladium® XP — 3
  - Power-Aware Emulation with DPA and CPF — 2
  - Acceleration and Emulation Using Palladium XP — 5
- Protium™ Rapid Prototyping Platform — 1.5

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- VHDL Language and Application (5)
- Verilog for VHDL Users (2)
- Real Modeling with Verilog AMS (2)
- Real Modeling with SystemVerilog AMS NEW (2)
- Verilog Language and Application (4)
- Master VHDL For Verilog Engineers (3)
- SystemVerilog for Design and Verification (5)
- SystemVerilog Advanced / Accelerated Verification Using UVM (5)
- SystemVerilog Advanced Register Verification Using UVM NEW (2)
- SystemVerilog Assertions (2)
- JasperGold® Formal Fundamentals NEW (3)
- Verification with PSL (2)
- C++ Language Fundamentals for Design and Verification (2)
- SystemC® Language Fundamentals (3)
- SystemC Synthesis with Stratus HLS NEW (3)
- SystemC Transaction-Level Modeling TLM2.0 (2)
- Perl for EDA Engineering (3)
- Tcl Scripting for EDA + Intro to Tk (3)

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Tensilica Processor IP Learning Map

Tensilica Processors

- Tensilica® Processor Fundamentals — 2 days, Online Course Available
- Tensilica Xtensa® Processor Interfaces — Online Course Available
- Tensilica Xtensa Hardware Verification and EDA — Online Course Available
- Tensilica Instruction Extension Language and Design — 1 day, Online Course Available
- Introduction to System Modeling with Tensilica Processor Cores — 1 day, Online Course Available

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine — 2 days, Online Course Available
- Tensilica ConnX BBE32EP Baseband Engine — 2 days, Online Course Available
- Tensilica ConnX BBE64EP Baseband Engine — 2 days, Online Course Available

Fusion DSP

- Tensilica Fusion F1 DSP — Online Course Available
- Tensilica Fusion G3 DSP — 2 days, Online Course Available
- Tensilica Fusion G6 DSP — 2 days, Online Course Available

HiFi Audio DSP

- Tensilica Audio Codec API — 0.5 days, Online Course Available
- Tensilica HiFi 2/EP/Mini Audio Engine ISA — Online Course Available
- Tensilica HiFi 3 Audio Engine ISA — 1 day, Online Course Available
- Tensilica HiFi 4 DSP — NEW — 1 day

Vision DSP

- Tensilica Vision P5 DSP — 2 days, Online Course Available
- Tensilica Vision P6 DSP — 2 days, Online Course Available
- Tensilica Vision C5 DSP — NEW — 1 day, Online Course Available

NEW New Course | # Number of days for instructor-led course | Online Course Available