Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# IC Package Design and Analysis Learning Map

## IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Skill Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
<td>Beginner</td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td>Beginner</td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro Package Designer Plus</td>
<td>Beginner</td>
</tr>
</tbody>
</table>

## SI/PI Analysis

<table>
<thead>
<tr>
<th>Course</th>
<th>Skill Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allegro Sigrity™ SI Foundations</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro Sigrity PI</td>
<td>Beginner</td>
</tr>
<tr>
<td>Sigiry PowerDC™ and OptimizePI™</td>
<td>Beginner</td>
</tr>
<tr>
<td>Sigiry SystemSI™ for Parallel Bus and Serial Link Analysis</td>
<td>Beginner</td>
</tr>
<tr>
<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
<td>Beginner</td>
</tr>
<tr>
<td>Clarity 3D Solver</td>
<td>Beginner</td>
</tr>
<tr>
<td>Celsius Thermal Solver</td>
<td>Beginner</td>
</tr>
</tbody>
</table>
Digital Design and Signoff Learning Map

Synthesis and Test

- Design For Test Fundamentals
- Virtuoso® Digital Implementation
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Stylus Common UI
- Test Synthesis with Genus Stylus Common UI
- Advanced Synthesis with Genus Stylus Common UI
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

Implementation

- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking

- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO

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System Design and Verification Learning Map

**Design and Verification Languages**

- Master VHDL For Verilog Engineers
- Real Modeling with Verilog AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
- Perl for EDA Engineering
- Tcl Scripting for EDA
- Verilog Language and Application
- VHDL Language and Application
- C++ Language Fundamentals for Design and Verification
- SystemC® Language Fundamentals
- SystemC Synthesis with Stratus HLS
- SystemC Transaction-Level Modeling TLM2.0
- SystemVerilog for Design and Verification
- Essential SystemVerilog for UVM (optional)
- SystemVerilog Accelerated Verification Using UVM
- UVM
- SystemVerilog Assertions
- SystemVerilog Assertions
- JasperGold® Formal Fundamentals
- SVA, Formal & JasperGold® Fundamentals for Designers
- SystemVerilog Advanced Register Verification Using UVM
- JasperGold® Formal Expert

**New Course**

- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available
- Digital Badge Available

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Tensilica Processor IP Learning Map

**Tensilica Xtensa NX**
- Tensilica® Xtensa® NX Processor Fundamentals
- Tensilica Xtensa NX Processor Interfaces
- Tensilica Instruction Extension Language and Design
- Tensilica System Modeling using XTSC

**ConnX DSP**
- Tensilica ConnX B10 DSP
- Tensilica ConnX B20 DSP

**Vision DSP**
- Tensilica Vision Q7 DSP

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