Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
  - Number of days: 3
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Design Entry Using OrCAD® Capture**
  - Number of days: 2
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro System Architect**
  - Number of days: 2
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Design Reuse**
  - Number of days: 1
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro AMS Simulator**
  - Number of days: 3
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

## PCB Design
- **Allegro PCB Editor Basic Techniques**
  - Number of days: 1
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro PCB Editor Intermediate Techniques**
  - Number of days: 2
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro PCB Router Basics**
  - Number of days: 2
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro PCB Editor Advanced Methodologies**
  - Number of days: 2
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Update Training**
  - Number of days: 2
  - Tiers of Cadence products used: 1
  - Online Course Available: Yes
  - Digital Badge Available: Yes

## SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
  - Number of days: 3
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Sigtry™ SI Foundations**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Sigtry PI**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Sigrity PowerDC™ and OptimizePI™**
  - Number of days: 1
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis**
  - Number of days: 3
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

## Library Development
- **Allegro PCB Librarian**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro EDM PCB Librarian**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Design Workbench for Administrators**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro PCB Editor SKILL Programming Language**
  - Number of days: 3
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Allegro Design Entry HDL SKILL® Programming Language**
  - Number of days: 3
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes

- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**
  - Number of days: 2
  - Tiers of Cadence products used: 2
  - Online Course Available: Yes
  - Digital Badge Available: Yes
## IC Package Design

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<td>Allegro® Package Designer</td>
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<tr>
<td>Allegro FPGA System Planner</td>
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<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
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<tr>
<td>OrbitIO™ System Planner</td>
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<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
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## SI/PI Analysis

<table>
<thead>
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<td>Allegro Sigrity PI</td>
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<td>Sigity PowerDC™ and OptimizePI™</td>
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<td>Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM</td>
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# Custom IC, Analog and RF Design Learning Map

## IC CAD

| SKILL® Language Programming Introduction | 2 | Beginner | 2 |
| SKILL Language Programming Fundamentals | 3 | | 3 |
| SKILL Language Programming | 5 | | 5 |
| SKILL Development of Parameterized Cells | 2 | | 2 |
| SKILL Programming for IC Layout Design | 2 | | 2 |
| Advanced SKILL Language Programming | 3 | | 3 |

## Layout Design and Advanced Nodes

### Virtuoso® Layout Design Basics

- Virtuoso® Connectivity-Driven Layout Transition
- Virtuoso® Layout Design Basics
- Virtuoso® Abstract Generator
- Virtuoso® Floorplanner
- Virtuoso® Space-Based Router
- Virtuoso® Space-Based Router Express

### Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands
- T2: Create and Edit Commands
- T3: Basic Commands
- T4: Advanced Commands
- T5: Interactive Routing
- T6: Constraint-Driven Flow and Power Routing
- T7: Module Generator and Floorplanner
- T8: Debugging Layout Issues

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### Virtuoso® Advanced-Node Series – ICADV

- T1: Place and Route
- T2: Electromigration

### Quantum™ QRC Transistor-Level Series

- Physical Verification System (PVS)
- T1: Overview and Technology Setup
- T2: Parasitic Extraction
- T3: Extracted View Flows and Advanced Features

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### Layout Verification

- Physical Verification Language Rules-Writer

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Digital Design and Signoff Learning Map

**Synthesis**
- Genus™ Synthesis Solution
- Low-Power Synthesis Flow with Genus Synthesis Solution
- Test Synthesis Using Genus Synthesis Solution
- Advanced Synthesis with Genus Synthesis Solution
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

**Implementation**
- Virtuoso® Digital Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO
- Conformal Constraint Designer

**Cadence® RTL-to-GDS Flow**

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