Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
# IC Package Design and Analysis Learning Map

## IC Package Design
- **SiP Layout**
- **Allegro® Package Designer**
- **Allegro FPGA System Planner**
- **Allegro Sigrity Package Assessment and Model Extraction**
- **OrbitIO™ System Planner**
- **Advanced Design Verification with the RAVEL Programming Language**

## SI/PI Analysis
- **Allegro Sigrity™ SI Foundations**
- **Allegro Sigrity PI**
- **Sigtry PowerDC™ and OptimizePI™**
- **Sigtry SystemSI™ for Parallel Bus and Serial Link Analysis**
- **Sigtry PowerSI® for Model Generation and Analysis**

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System Design and Verification Learning Map

Simulation, Acceleration, Coverage and Debug

- Incisive® SystemC®, VHDL, and Verilog Simulation
- Incisive Comprehensive Coverage with IMC
- Incisive Simulation Performance Optimization
- Perspec™ System Verifier
- Indago™ Analyzer App (15.2)
- Low-Power Simulation with CPF
- Low-Power Simulation with IEEE1801 UPF
- Incisive Functional Safety Simulator
- Xcelium™ Simulator
- Cadence® RTL-To-GDSII Flow
- Foundations of Metric-Driven Verification
- Xcelium Integrated Coverage
- Indago Analyzer App (17.10)
- Metric-Driven Verification Using vManager™
- vManager Tool Usage in Batch Mode
- Specman® Fundamentals for Block-level Environment Developers
- Specman Advanced Verification
- VIP Basic Building Blocks and Usage

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