

# Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

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- [IC Package Design and Analysis](#)
- [Custom Design with Virtuoso® Technology](#)
- [Digital Design and Signoff](#)
- [System Design and Analysis](#)
- [Tensilica® Processor IP](#)

# Learning Map for PCB Design and Analysis

## Logic Design

## PCB Design

## SI/PI Analysis

## Library Development

	Logic Design	PCB Design	SI/PI Analysis	Library Development	
Analog Focus	<p><a href="#">Allegro® AMS Simulator Adv. Analysis (1)</a> <sup>EE</sup></p> <p><a href="#">Allegro AMS Simulator (3)</a></p> <p><a href="#">PSpice® Advanced Analysis (1)</a></p> <p><a href="#">Analog Simulation with PSpice (3)</a></p>				
Master	<p><a href="#">Allegro FPGA System Planner (2)</a></p>	<p><sup>NEW</sup> <a href="#">Allegro PCB Editor Advanced Methodologies (1)</a></p>	<p><a href="#">Allegro Sigrity™ System Serial Link Analysis (1)</a></p> <p><a href="#">Sigrity PowerSI® for Model Generation and Analysis (2)</a></p>	<p><a href="#">Allegro PCB Editor SKILL® Language (3)</a></p> <p><a href="#">Allegro Design Entry HDL SKILL Language (3)</a></p>	
Experienced	<p><a href="#">Allegro Design Reuse (1)</a> <sup>EE</sup></p> <p><a href="#">Allegro System Architect (1)</a></p> <p><a href="#">Allegro Design Workbench for Engineers and Designers (1)</a></p> <p><a href="#">Allegro Team Design Authoring (1)</a></p>	<p><a href="#">Allegro PCB Router Basics (2)</a></p>	<p><a href="#">Allegro Sigrity Power-Aware Parallel Bus Analysis (2)</a></p> <p><a href="#">Sigrity PowerDC™ and OptimizePI™ (1)</a></p>	<p><a href="#">Allegro Design Workbench for Administrators (2)</a></p>	
<p><a href="#">Allegro High-Speed Constraint Management (2)</a> <sup>EE</sup></p> <p><a href="#">Allegro Tool Setup and Configuration (2)</a></p>					
Core	<p><a href="#">Allegro Design Entry HDL Basics (1)</a></p> <p><a href="#">Allegro Design Entry HDL Front-to-Back Flow (3)</a></p>	<p><a href="#">Allegro Design Entry Using OrCAD® Capture (2)</a></p> <p><a href="#">OrCAD CIS (1)</a></p>	<p><a href="#">Allegro PCB Editor Intermediate Techniques (2)</a></p> <p><a href="#">Allegro PCB Editor Basic Techniques (3)</a></p>	<p><a href="#">Allegro Sigrity PI (1)</a></p> <p><a href="#">Allegro Sigrity SI Foundations (2)</a></p> <p><a href="#">PCB Design at RF - multi-Gigabit Transmission, EMI Control, and PCB Materials(2)</a></p> <p><a href="#">Essential High-speed PCB Design for Signal Integrity(3)</a></p>	<p><a href="#">Allegro PCB Librarian (2)</a></p> <p><a href="#">Allegro Design Workbench for Librarians (2)</a></p>

▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). <sup>NEW</sup> New course (see course catalog at cadence.com for a complete course listing).

# Learning Map for IC Package Design and Analysis

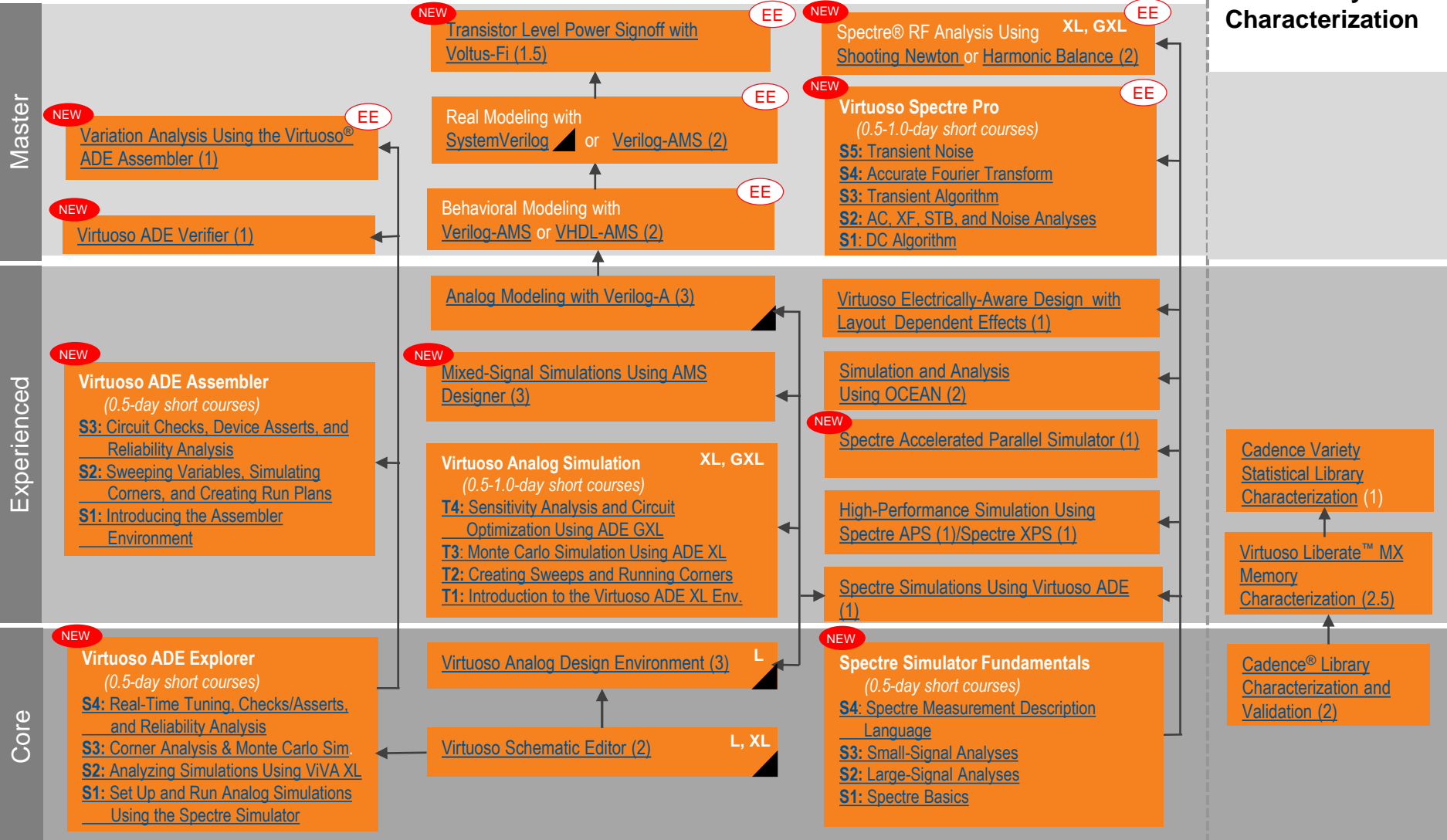
	SI/PI Analysis	IC Package Design
Analog Focus		
Master	<ul style="list-style-type: none"> <li><a href="#">Allegro® Sigrity™ System Serial Link Analysis (1)</a></li> <li><a href="#">Sigrity PowerSI® for Model Generation and Analysis (2)</a></li> </ul>	
Experienced	<ul style="list-style-type: none"> <li><a href="#">Allegro Sigrity Power-Aware Parallel Bus Analysis (2)</a></li> <li><a href="#">Sigrity PowerDC™ and OptimizePI™ (1)</a></li> </ul>	<ul style="list-style-type: none"> <li><a href="#">OrbitIO™ System Planner (1)</a></li> <li><a href="#">Allegro Sigrity Package Assessment and Model Extraction (1)</a></li> </ul>
	<a href="#">Allegro High-Speed Constraint Management (2)</a>	
	<a href="#">Allegro Tool Setup and Configuration (2)</a>	
Core	<ul style="list-style-type: none"> <li><a href="#">Allegro Sigrity PI (1)</a></li> <li><a href="#">Allegro Sigrity SI Foundations (2)</a></li> </ul>	<ul style="list-style-type: none"> <li><a href="#">Allegro Package Designer (4)</a></li> <li><a href="#">SiP Layout (5)</a></li> </ul>

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# Learning Map for Custom Design with Virtuoso Technology – Custom IC, Analog and RF Design

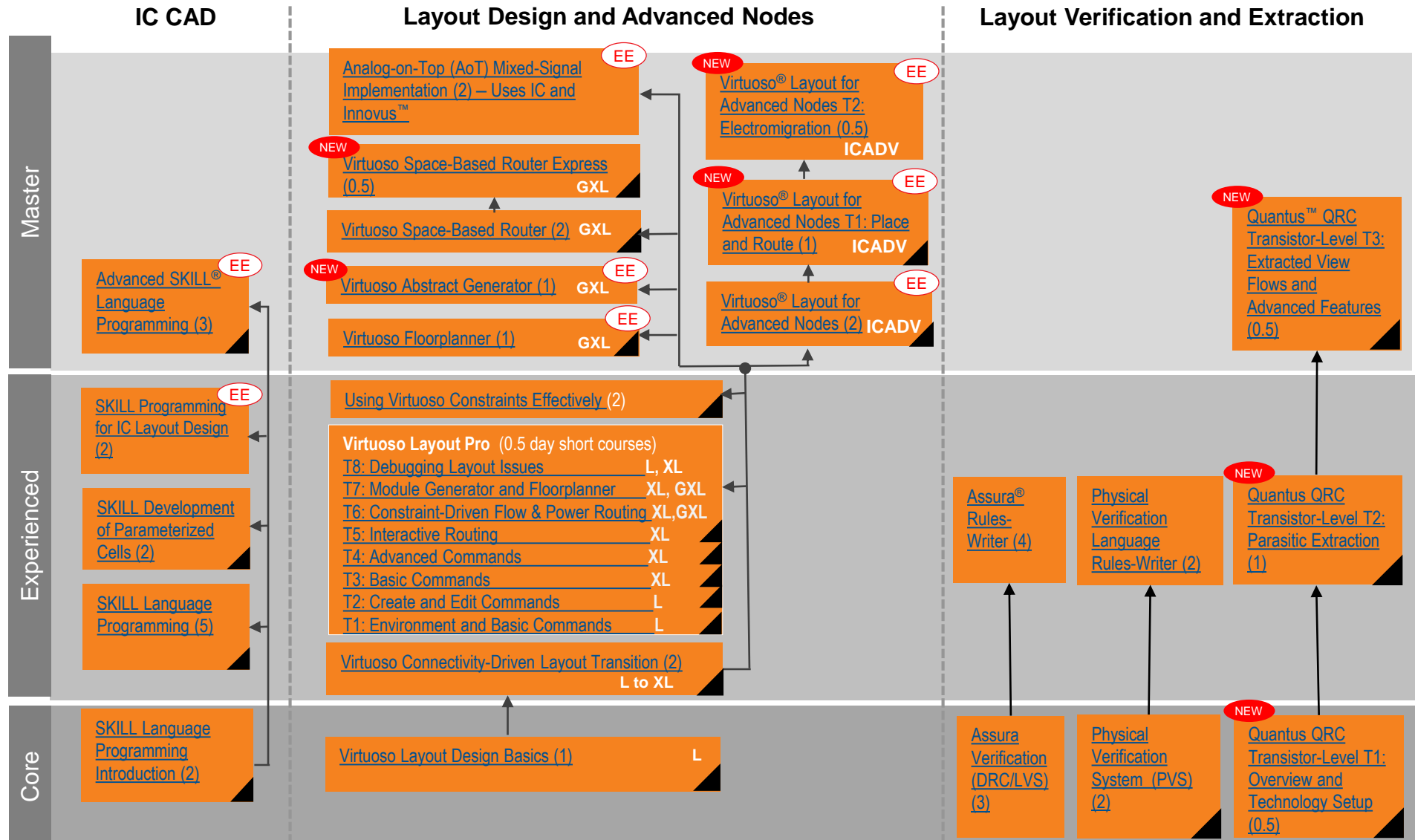
## Circuit Design, Simulation, Modeling and RF Design

## Library Characterization



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# Learning Map for Custom Design with Virtuoso Technology – Custom IC, Analog and RF Design



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# Learning Map for Digital Design and Signoff

## Synthesis

## Implementation

## Silicon Signoff

## Equivalence Checking

Master

[Advanced Synthesis with Genus™ Synthesis Solution \(1\)](#) <sup>EE</sup>

Experienced

[Modus® Test Solution \(1\)](#)

[Test Synthesis Using Genus Synthesis Solution \(2\)](#)

[Low-Power Synthesis Flow with Genus Synthesis Solution \(1\)](#) <sup>EE</sup>

[Fundamentals of IEEE 1801 Low-Power Specification Format \(1\)](#) <sup>EE</sup>

[Joules™ Power Calculator \(1\)](#) <sup>EE</sup>

[Analog-on-Top Mixed-Signal Implementation \(2\)](#) <sup>EE</sup>

[Low-Power Flow with Innovus™ Implementation System \(1\)](#) <sup>EE</sup>

[Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis \(1\)](#)

[Innovus Implementation System \(Hierarchical\) \(1\)](#)

[Voltus™ Power-Grid Analysis and Signoff \(2\)](#) <sup>XL EE</sup>

[Conformal® ECO \(1\)](#)

[Low-Power Verification with Conformal \(1\)](#)

Core

[Genus Synthesis Solution \(2\)](#)

[Innovus Implementation System \(Block\) \(3\)](#)

[Virtuoso® Digital Implementation \(2\)](#)

[Tempus™ Signoff Timing Analysis and Closure \(2\)](#) <sup>XL</sup>

[Basic Static Timing Analysis \(2\)](#)

[Logic Equivalence Checking with Conformal EC \(2\)](#)

[Cadence RTL-to-GDSII Flow \(2\)](#)

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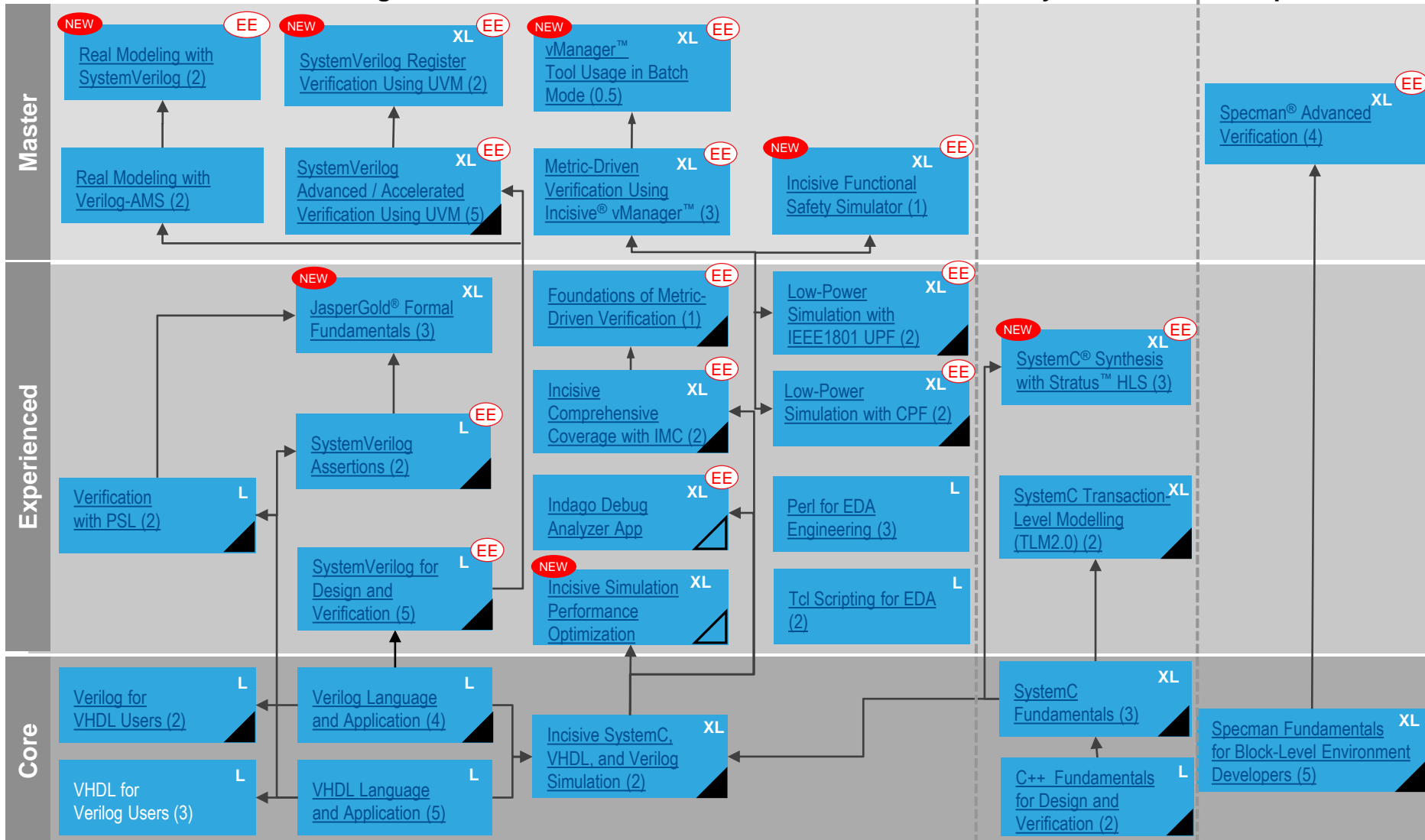


# Learning Map for System Design and Verification – Languages, Methodologies, and Tools

## HDL Design and Verification with Incisive

## SystemC

## Specman

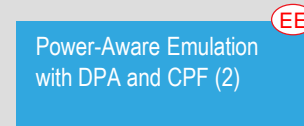
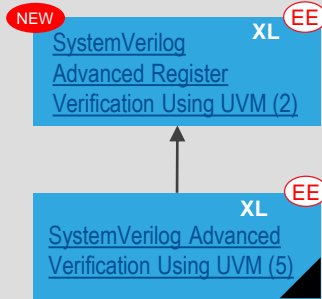


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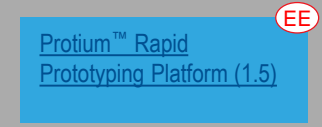
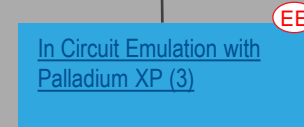
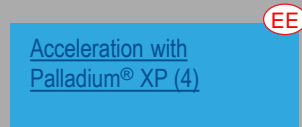
## Acceleration

## Emulation

Experienced



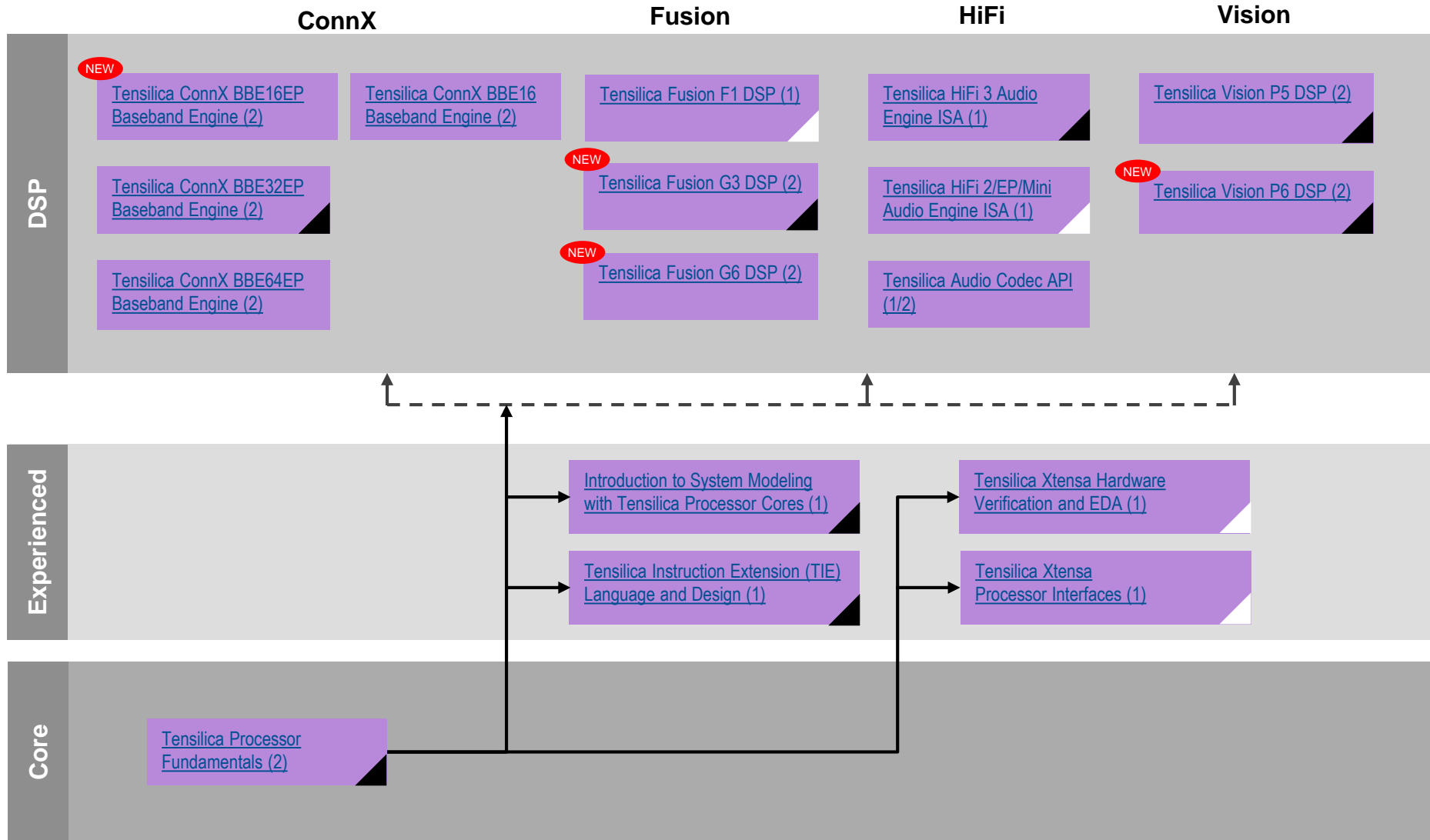
Core



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# Learning Map for Tensilica Processor IP



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