Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
### PCB Design and Analysis Learning Map

**Logic Design**
- **Allegro® Design Entry HDL Front-to-Back Flow**
- **Allegro Design Entry HDL Basics**
- **Allegro System Design Authoring**
- **Allegro Design Reuse**
- **Allegro AMS Simulator**
- **Allegro AMS Simulator Advanced Analysis**

**PCB Design**
- **Allegro Design Entry Using OrCAD® Capture**
- **OrCAD CIS**
- **Allegro EDM Design Entry HDL Front-to-Back Flow**
- **Allegro Team Design Authoring**
- **Allegro EDM for Engineers and Designers**
- **Analog Simulation with PSpice®**
- **Advanced Simulation with PSpice Advanced Analysis**

**SI/PI Analysis**
- **Allegro PCB Editor Basic Techniques**
- **Allegro PCB Editor Intermediate Techniques**
- **Allegro PCB Router Basics**
- **Allegro PCB Editor Advanced Methodologies**
- **Allegro High-Speed Constraint Management**
- **Allegro Update Training**

**Library Development**
- **Essential High-Speed PCB Design for Signal Integrity**
- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
- **Allegro Sigry™ SI Foundations**
- **Allegro Sigry™ PI**
- **Sigry PowerDC™ and OptimizePI™**
- **Sigry SystemSI™ for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**

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# IC Package Design and Analysis Learning Map

## IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Number of Days</th>
<th>Cadence Products Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td>4</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td>4</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td>2</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
<td>1</td>
<td>Beginner</td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td>1</td>
<td>Beginner</td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td>2</td>
<td>Beginner</td>
</tr>
</tbody>
</table>

## SI/PI Analysis

<table>
<thead>
<tr>
<th>Course</th>
<th>Number of Days</th>
<th>Cadence Products Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allegro Sigrity™ SI Foundations</td>
<td>2</td>
<td>Beginner</td>
</tr>
<tr>
<td>Allegro Sigrity PI</td>
<td>1</td>
<td>Beginner</td>
</tr>
<tr>
<td>Sigirty PowerDC™ and OptimizePI™</td>
<td>1</td>
<td>Beginner</td>
</tr>
<tr>
<td>Sigirty SystemSI™ for Parallel Bus and Serial Link Analysis</td>
<td>3</td>
<td>Beginner</td>
</tr>
<tr>
<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
<td>2</td>
<td>Beginner</td>
</tr>
</tbody>
</table>

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Digital Design and Signoff Learning Map

Synthesis and Test
- Design For Test Fundamentals
  - Virtuoso® Digital Implementation
    - Genus™ Synthesis Solution with Stylus Common UI
    - Low-Power Synthesis Flow with Genus Synthesis Solution
    - Test Synthesis Using Genus Synthesis Solution
    - Advanced Synthesis with Genus Stylus Common UI
    - Fundamentals of IEEE 1801 Low-Power Specification Format
    - Modus DFT Software Solution
    - Joules™ Power Calculator

Implementation
- Innovus Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

Silicon Signoff
- Basic Static Timing Analysis
  - Tempus™ Signoff Timing Analysis and Closure
  - Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking
- Conformal® Equivalence Checking
  - Conformal Low-Power Verification
  - Conformal ECO
  - Conformal Constraint Designer

Cadence® RTL-to-GDSII Flow

New Course 8 Number of days for instructor-led course Online Course Available Digital Badge Available

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