Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
## PCB Design and Analysis Learning Map

### Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
- **Allegro Design Entry HDL Basics**
- **Allegro System Architect**
- **Allegro Design Reuse**
- **Allegro AMS Simulator**
- **Analog Simulation with PSpice®**

### PCB Design
- **Allegro Design Entry Using OrCAD® Capture**
- **OrCAD CIS**
- **Allegro EDM Design Entry HDL Front-to-Back Flow**
- **Allegro Team Design Authoring**
- **Allegro EDM for Engineers and Designers**
- **Analog Simulation with PSpice Advanced Analysis**
- **Advanced Design Verification with the RAVEL Programming Language**
- **Allegro PCB Editor Basic Techniques**
- **Allegro PCB Editor Intermediate Techniques**
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- **Allegro High-Speed Constraint Management**
- **Allegro Update Training**

### SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
- **Allegro Sigrity™ SI Foundations**
- **Allegro Sigrity PI**
- **Sigrity PowerDC™ and OptimizePI™**
- **Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**

### Library Development
- **Allegro PCB Librarian**
- **Allegro EDM PCB Librarian**
- **Allegro EDM for Administrators**
- **Allegro EDM Administration for OrCAD**
- **Allegro Design Entry HDL SKILL® Programming Language**
- **Allegro PCB Editor SKILL Programming Language**

**Legend:**
- **NEW** New Course
- **Number of days for instructor-led course**
- **Tiers of Cadence products used in course**
- **Online Course Available**
- **Digital Badge Available**

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System Design and Verification Learning Map

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- **Verilog Language and Application**
  - Master VHDL For Verilog Engineers
    - SystemVerilog Advanced / Accelerated Verification Using UVM
      - SystemVerilog Advanced Register Verification Using UVM
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  - SystemVerilog for Design and Verification
    - SystemVerilog Advanced / Accelerated Verification Using UVM
      - SystemVerilog Advanced Register Verification Using UVM
        - New Course
- **VHDL Language and Application**
  - Verilog for VHDL Users
    - Verification with PSL
      - JasperGold® Formal Fundamentals
        - New Course
  - SystemVerilog for Design and Verification
    - SystemVerilog Assertions
      - Verification with PSL
        - JasperGold® Formal Fundamentals
          - New Course
- **C++ Language Fundamentals for Design and Verification**
  - SystemC® Language Fundamentals
    - SystemC Synthesis with Stratus HLS
      - SystemC Transaction-Level Modeling TLM2.0
        - Perl for EDA Engineering
          - Tcl Scripting for EDA + Intro to Tk

Number of days for instructor-led course

Tiers of Cadence products used in course

Online Course Available

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