Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
### PCB Design and Analysis Learning Map

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**Notes:**
- **New Course:** Indicates a new course.
- **Number of days for instructor-led course:** Indicates the duration of the course.
- **Tiers of Cadence products used in course:** Indicates the levels of Cadence products used in the course.
- **Online Course Available:** Indicates if the course is available online.
- **Digital Badge Available:** Indicates if a digital badge is available for completion.

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# IC Package Design and Analysis Learning Map

## IC Package Design

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- New: Indicates a new course.
- Days: Number of days for instructor-led course.
- Tiers of Cadence products used in course.
- Online Course Available.
System Design and Verification Learning Map

Simulation, Acceleration, Coverage and Debug

- Incisive® SystemC®, VHDL, and Verilog Simulation
- Xcelium™ Simulator
- Cadence® RTL-To-GDSII Flow
- Foundations of Metric-Driven Verification
- Xcelium Integrated Coverage
- Indago™ Debug Analyzer App
- Metric-Driven Verification Using vManager™
- vManager Tool Usage in Batch Mode
- Specman® Fundamentals for Block-level Environment Developers
- Specman Advanced Verification
- VIP Basic Building Blocks and Usage

New Course
Number of days for instructor-led course
Tiers of Cadence products used in course
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System Design and Verification Learning Map

Design and Verification Languages

- **Verilog Language and Application**
  - Master VHDL For Verilog Engineers
  - SystemVerilog for Design and Verification
  - SystemVerilog Advanced / Accelerated Verification Using UVM
  - SystemVerilog Advanced Register Verification Using UVM

- **VHDL Language and Application**
  - Verilog for VHDL Users
  - SystemVerilog Assertions
  - JasperGold® Formal Fundamentals

- **C++ Language Fundamentals for Design and Verification**
  - SystemC® Language Fundamentals
  - SystemC Synthesis with Stratus HLS
  - SystemC Transaction-Level Modeling TLM2.0
  - Perl for EDA Engineering
  - Tcl Scripting for EDA + Intro to Tk

**New Course**

- **Number of days for instructor-led course**
- **Tiers of Cadence products used in course**
- **Online Course Available**

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