Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
## PCB Design and Analysis Learning Map

### Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
- **Allegro Design Entry Using OrCAD® Capture**
- **OrCAD CIS**
- **OrCAD Capture Constraint Manager PCB Flow**
- **Allegro System Capture**
- **Allegro System Architect**
- **Allegro Design Reuse**
- **Allegro AMS Simulator**
- **Allegro AMS Simulator Advanced Analysis**

### PCB Design
- **Allegro PCB Editor Basic Techniques**
- **Allegro PCB Editor Intermediate Techniques**
- **Allegro PCB Router Basics**
- **Allegro PCB Editor Advanced Methodologies**
- **Allegro High-Speed Constraint Management**
- **Advanced Design Verification with the RAVEL Programming Language**

### SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
- **Allegro SigtryTM SI Foundations**
- **Allegro Sigtry PI**
- **Sigrity PowerDC™ and OptimizePI™**
- **Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**
- **Clarity 3D Solver**

### Library Development
- **Allegro PCB Librarian**
- **Allegro EDM PCB Librarian**
- **Allegro EDM for Administrators**
- **Allegro EDM Administration for OrCAD**
- **Allegro Design Entry HDL SKILL® Programming Language**
- **Allegro PCB Editor SKILL Programming Language**

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**New Course**
**Number of days for instructor-led course**
**Tiers of Cadence products used in course**
**Online Course Available**
**Digital Badge Available**
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# IC Package Design and Analysis Learning Map

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Digital Design and Signoff Learning Map

**Synthesis and Test**
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Stylus Common UI
  - Test Synthesis with Genus Stylus Common UI
  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

**Implementation**
- Innovus™ Implementation System (Block)
  - Innovus Implementation System (Hierarchical)
  - Low-Power Flow with Innovus Implementation System
  - Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

**Silicon Signoff**
- Basic Static Timing Analysis
  - Tempus™ Signoff Timing Analysis and Closure
  - Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Conformal® Equivalence Checking
  - Conformal Low-Power Verification
  - Conformal ECO

**Cadence® RTL-to-GDSII Flow**

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System Design and Verification Learning Map

Simulation, Coverage and Debug

Xcelium™ Simulator

Cadence® RTL-To-GDSII Flow

VIP Basic Building Blocks and Usage

Low-Power Simulation with CPF

Low-Power Simulation with IEEE1801 UPF

Foundations of Metric-Driven Verification

Xcelium Integrated Coverage

Metric-Driven Verification Using vManager™

vManager Tool Usage in Batch Mode

Indago™ Debug Analyzer App

Perspec™ System Verifier - Basic

Incisive Functional Safety Simulator

Specman® Fundamentals for Block-Level Environment Developers

Specman® Advanced Verification

VIP Basic Building Blocks and Usage

Low-Power Simulation with CPF

Low-Power Simulation with IEEE1801 UPF

Foundations of Metric-Driven Verification

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