Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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Digital Design and Signoff Learning Map

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- Virtuoso® Digital Implementation
  - Genus™ Synthesis Solution with Stylus Common UI
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  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

Silicon Signoff
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO
- Conformal Constraint Designer

Cadence® RTL-to-GDSII Flow

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