

Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

PCB Design and Analysis Learning Map




















Beginner

Advanced















Beginner

Advanced

Logic Design

Allegro® Design Entry HDL Front-to-Back Flow  	Allegro Design Entry Using OrCAD® Capture  
Allegro Design Entry HDL Basics  	OrCAD CIS 
Allegro System Design Authoring   NEW	
Allegro System Architect  	Allegro Team Design Authoring  
Allegro Design Reuse  	Allegro Design Workbench for Engineers and Designers  
Allegro AMS Simulator 	Analog Simulation with PSpice®  
Allegro AMS Simulator Advanced Analysis  	Analog Simulation with PSpice Advanced Analysis  











PCB Design

Allegro PCB Editor Basic Techniques  
Allegro PCB Editor Intermediate Techniques  
Allegro PCB Router Basics  
Allegro PCB Editor Advanced Methodologies   NEW
Allegro High-Speed Constraint Management  
Allegro Update Training   NEW
Advanced Design Verification with the RAVEL Programming Language   NEW

SI/PI Analysis

Essential High-Speed PCB Design for Signal Integrity 
PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials 
Allegro Sigrity™ SI Foundations  
Allegro Sigrity PI  
Sigrity PowerDC™ and OptimizePI™  
Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis   NEW
Sigrity PowerSI® for Model Generation and Analysis  

Library Development

Allegro PCB Librarian  
Allegro Design Workbench for Librarians 
Allegro Design Workbench for Administrators 
Allegro Design Entry HDL SKILL® Programming  
Allegro PCB Editor SKILL Programming Language  
Allegro Tool Setup and Configuration  

IC Package Design and Analysis Learning Map

Beginner



Advanced

IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis **NEW**



Sigrity PowerSI® for Model Generation and Analysis



Beginner



Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

Beginner

Advanced

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

Virtuoso® Analog Design Environment



Virtuoso Analog Simulation Series NEW

- T1: Introduction to the Virtuoso ADE XL Environment** XL 1
- T2: Creating Sweeps and Running Corners** XL 0.5
- T3: Monte Carlo Simulation Using ADE XL** XL 0.5
- T4: Sensitivity Analysis and Circuit Optimization Using ADE GXL** GXL 0.5

Mixed-Signal Simulations Using AMS Designer 3

Analog Modeling with Verilog-A 3

Behavioral Modeling with / Verilog-AMS / VHDL-AMS 2

Real Modeling with / SystemVerilog / Verilog-AMS NEW 2

Transistor-Level Power Signoff with Voltus™-Fi NEW 1.5

Virtuoso Schematic Editor



Virtuoso® ADE Explorer Series NEW

- S1: Set Up and Run Analog Simulations Using the Spectre® Simulator** 0.5
- S2: Analyzing Simulations Using ViVA XL** 0.5
- S3: Corner Analysis and Monte Carlo Simulation** 0.5
- S4: Real-Time Tuning, Checks/Asserts, and Reliability Analysis** 0.5

Virtuoso ADE Assembler Series NEW

- S1: Introducing the Assembler Environment** 0.5
- S2: Sweeping Variables, Simulating Corners and Creating Run Plans** 0.5
- S3: Circuit Checks, Device Asserts and Reliability Analysis** 0.5

Virtuoso ADE Verifier NEW 1

Variation Analysis Using the Virtuoso Variation Option NEW 1

Spectre Simulator Fundamentals Series NEW

- S1: Spectre Basics** 0.5
- S2: Large-Signal** 0.5
- S3: Small-Signal** 0.5
- S4: Spectre MDL** 0.5

High-Performance Sim. using Spectre Simulators 2

Spectre Accelerated Parallel Simulator (APS) NEW 1

Spectre XPS for Mixed-Signal Designs NEW 1

Virtuoso EAD with LDE 1

Virtuoso Spectre Pro Series

- S1: DC Algorithm** 0.5
- S2: AC, XF, STB, Noise** 0.5
- S3: Transient Algorithm** 0.5
- S4: Fourier Transform** 0.5
- S5: Transient Noise** 1

Spectre® RF/ Shooting Newton / Harmonic Balance 2

Library Characterization

Cadence® Library Characterization and Validation 2

Virtuoso Liberate™ MX for Memory Characterization 2.5

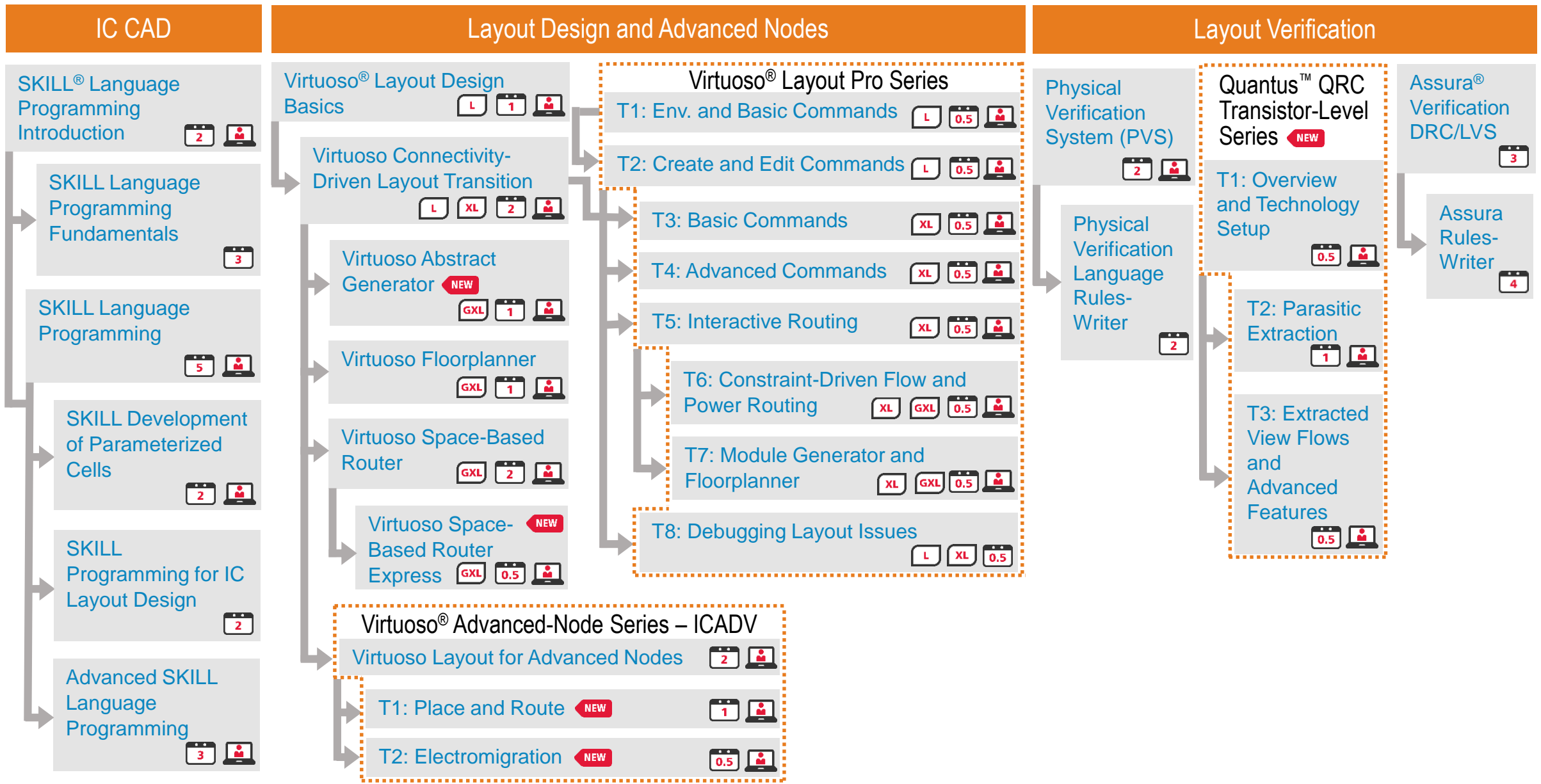
Cadence Variety™ Statistical Library Characterization 1

Beginner

Advanced

Beginner

Advanced



Digital Design and Signoff Learning Map

Beginner

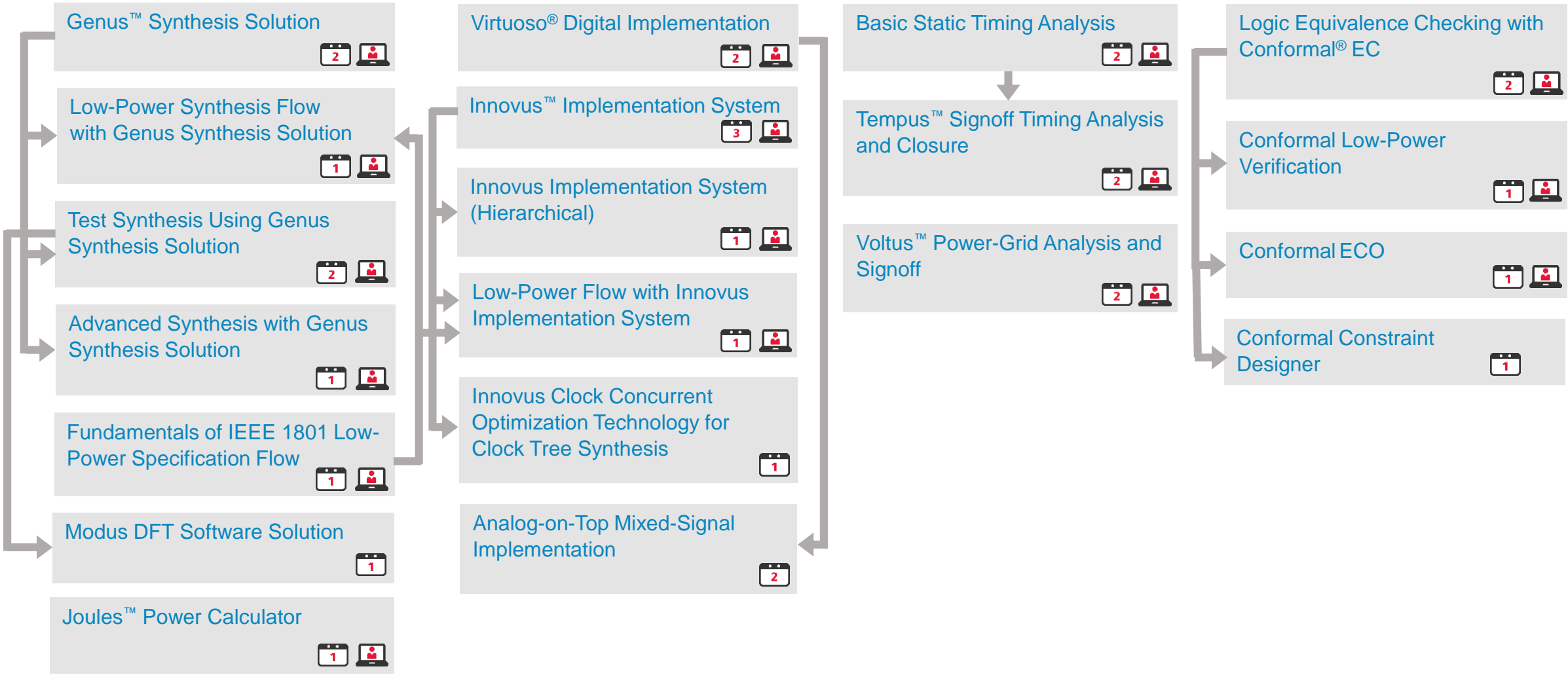
Advanced

Beginner

Advanced

Synthesis Implementation Silicon Signoff Equivalence Checking

Cadence® RTL-to-GDS Flow 2



System Design and Verification Learning Map

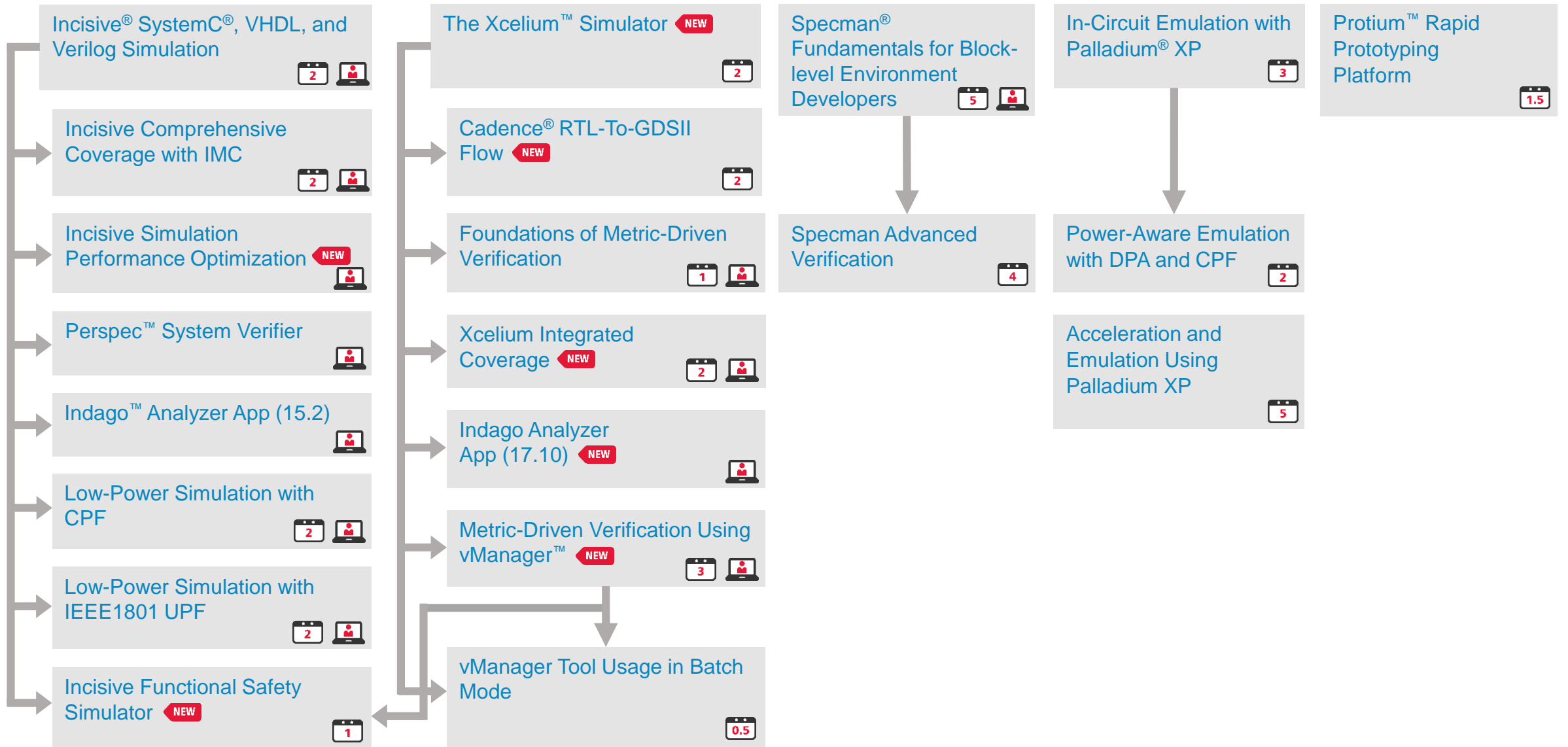
Beginner

Advanced

Beginner

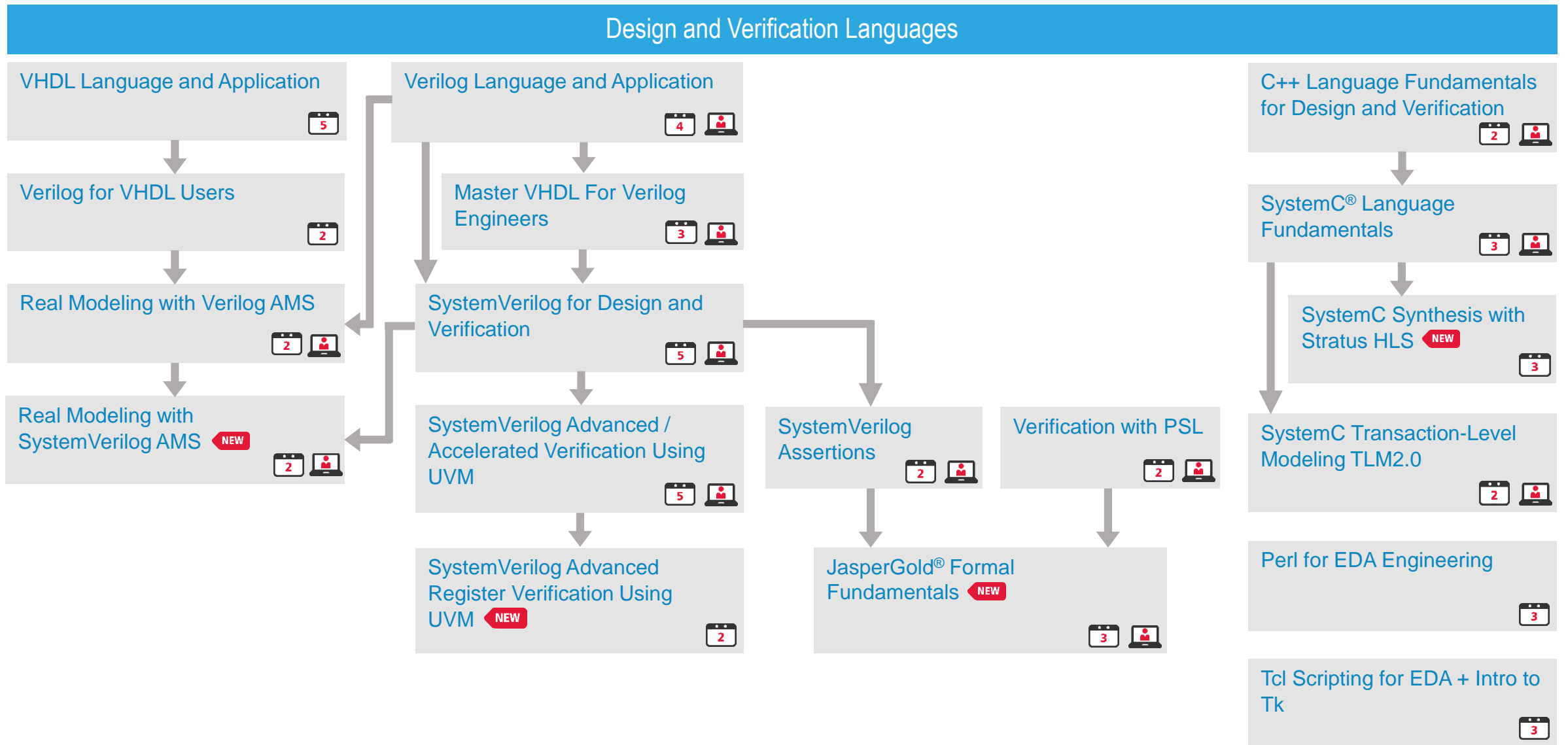
Advanced

Simulation, Acceleration, Emulation, Coverage and Debug



System Design and Verification Learning Map

Beginner



Beginner

Advanced

Tensilica Processor IP Learning Map

Tensilica Processors

Tensilica® Processor Fundamentals



ConnX DSP

Fusion DSP

HiFi Audio DSP

Vision DSP

Tensilica Xtensa® Processor Interfaces



Tensilica Xtensa Hardware Verification and EDA



Tensilica Instruction Extension Language and Design



Introduction to System Modeling with Tensilica Processor Cores



Tensilica ConnX BBE16EP Baseband Engine



Tensilica ConnX BBE32EP Baseband Engine



Tensilica ConnX BBE64EP Baseband Engine



Tensilica Fusion F1 DSP



Tensilica Fusion G3 DSP



Tensilica Fusion G6 DSP



Tensilica Audio Codec API



Tensilica HiFi 2/EP/Mini Audio Engine ISA



Tensilica HiFi 3 Audio Engine ISA



Tensilica HiFi 4 DSP **NEW**



Tensilica Vision P5 DSP



Tensilica Vision P6 DSP



Tensilica Vision C5 DSP **NEW**



New Course



Number of days for instructor-led course



Online Course Available

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