Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# IC Package Design and Analysis Learning Map

## IC Package Design

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<td>Allegro® Package Designer</td>
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<td>Allegro FPGA System Planner</td>
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<td>Allegro Sigrity Package Assessment and Model Extraction</td>
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<td>OrbitIO™ System Planner</td>
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<td>Advanced Design Verification with the RAVEL Programming Language</td>
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## SI/PI Analysis

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<td>Celsius Thermal Solver</td>
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Custom IC, Analog and RF Design Learning Map

Circuit Design, Simulation, Modeling and RF Design

Analog Modeling with Verilog-A
- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model
- Behavioral Modeling with Verilog AMS
- Behavioral Modeling with VHDL-AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

Virtuoso Schematic Editor
Virtuoso Visualization and Analysis
Virtuoso® ADE Explorer & Assembler Series
- ADE Explorer & Single Test Corner Analysis
- ADE Assembler & Multi Test Corner Analysis
- Sweeping Variables and Simulating Corners
- Monte Carlo, Real-Time Tuning & Run Plans

Virtuoso® ADE Verifier Series
- Setup, Run, & View Verifier Results
- Reference Flow and Analog Coverage Using the Setup Library Assistant

Design Checks and Asserts

5G mmWave Handset System Design – RFIC (Transceiver) Design

Spectre® Simulator Fundamentals Series
- S1 Spectre Basics
- S2 Large-Signal
- S3 Small-Signal
- S4 Spectre MDL

Spectre Accelerated Parallel Simulator (APS)

Spectre XPS for Mixed-Signal Designs

Virtuoso® Spectre® Pro Series
- S1 DC Algorithm
- S2 AC, XF, STB, Noise
- S3 Transient Algorithm
- S4 Fourier Transform
- S5 Transient Noise

Spectre® RF Shooting Newton
Spectre® RF Harmonic Balance

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Digital Design and Signoff Learning Map

**Synthesis and Test**
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Stylus Common UI
- Test Synthesis with Genus Stylus Common UI
- Advanced Synthesis with Genus Stylus Common UI
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

**Implementation**
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal Low-Power Verification Using IEEE1801
- Conformal ECO