Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
# IC Package Design and Analysis Learning Map

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- **New Course**
- **Number of days for instructor-led course**
- **Tiers of Cadence products used in course**
- **Online Course Available**
Custom IC, Analog and RF Design Learning Map

**IC CAD**
- SKILL Language Programming Introduction
- SKILL Language Programming Fundamentals
- SKILL Language Programming
- SKILL Development of Parameterized Cells
- SKILL Programming for IC Layout Design
- Advanced SKILL Language Programming

**Layout Design and Advanced Nodes**
- Virtuoso® Layout Design Basics
- Virtuoso® Connectivity-Driven Layout Transition
- Virtuoso Abstract Generator
- Virtuoso Floorplanner
- Virtuoso Space-Based Router
- Virtuoso Space-Based Router Express
- Virtuoso® Advanced-Node Series – ICADV
  - Virtuoso Layout for Advanced Nodes
    - T1: Place and Route
    - T2: Electromigration

**Virtuoso® Layout Pro Series**
- T1: Env. and Basic Commands
- T2: Create and Edit Commands
- T3: Basic Commands
- T4: Advanced Commands
- T5: Interactive Routing
- T6: Constraint-Driven Flow and Power Routing
- T7: Module Generator and Floorplanner
- T8: Debugging Layout Issues

**Layout Verification**
- Physical Verification System (PVS)
- Physical Verification Language Rules-Writer
- Quantumus Extraction Solution
  - Transistor-Level Series
- T1: Overview and Technology Setup
- T2: Parasitic Extraction
- T3: Extracted View Flows and Advanced Features
# Digital Design and Signoff Learning Map

## Synthesis and Test
- **Design For Test Fundamentals**
- **Virtuoso® Digital Implementation**
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Synthesis Solution
- **Test Synthesis Using Genus Synthesis Solution**
- **Advanced Synthesis with Genus Stylus Common UI**
- **Fundamentals of IEEE 1801 Low-Power Specification Format**
- **Modus DFT Software Solution**
- **Joules™ Power Calculator**

## Implementation
- **Innovus™ Implementation System**
  - (Block)
- **Innovus Implementation System** (Hierarchical)
  - Low-Power Flow with Innovus Implementation System
- **Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis**
- **Analog-on-Top Mixed-Signal Implementation**

## Silicon Signoff
- **Basic Static Timing Analysis**
- **Tempus™ Signoff Timing Analysis and Closure**
- **Voltus™ Power-Grid Analysis and Signoff**

## Equivalence Checking
- **Conformal® Equivalence Checking**
- **Conformal Low-Power Verification**
- **Conformal ECO**
- **Conformal Constraint Designer**

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**Cadence® RTL-to-GDS Flow**

- **Cadence® RTL-to-GDS Flow**
- **New Course**
- **Number of days for instructor-led course**
- **Online Course Available**
- **Digital Badge Available**

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