

Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- [PCB Design and Analysis](#)
- [IC Package Design and Analysis](#)
- [Custom Design with Virtuoso® Technology](#)
- [Digital Design and Signoff](#)
- [System Design and Analysis](#)
- [Tensilica® Processor IP](#)

Learning Map for PCB Design and Analysis

Logic Design

PCB Design

SI/PI Analysis

Library Development

	Logic Design	PCB Design	SI/PI Analysis	Library Development
Analog Focus	<p>Allegro® AMS Simulator Adv. Analysis (1) ^(EE)</p> <p>Allegro AMS Simulator (3)</p> <p>PSpice® Advanced Analysis (1)</p> <p>Analog Simulation with PSpice (3)</p>			
Master	<p>Allegro FPGA System Planner (2)</p>	<p>^(NEW) Allegro PCB Editor Advanced Methodologies (1)</p>	<p>Allegro Sigrity™ System Serial Link Analysis (1)</p> <p>Sigrity PowerSI® for Model Generation and Analysis (2)</p>	<p>Allegro PCB Editor SKILL® Language (3)</p> <p>Allegro Design Entry HDL SKILL Language (3)</p>
Experienced	<p>Allegro Design Reuse (1) ^(EE)</p> <p>Allegro System Architect (1)</p> <p>Allegro Design Workbench for Engineers and Designers (1)</p> <p>Allegro Team Design Authoring (1)</p>	<p>Allegro PCB Editor Miniaturization Option (1)</p> <p>Allegro PCB Router Basics (2)</p>	<p>Allegro Sigrity Power-Aware Parallel Bus Analysis (2)</p> <p>Sigrity PowerDC™ and OptimizePI™ (1)</p>	<p>Allegro Design Workbench for Administrators (2)</p>
<p>Allegro High-Speed Constraint Management (2) ^(EE)</p> <p>Allegro Tool Setup and Configuration (2)</p>				
Core	<p>Allegro Design Entry HDL Basics (1)</p> <p>Allegro Design Entry HDL Front-to-Back Flow (3)</p>	<p>Allegro Design Entry Using OrCAD® Capture (2)</p> <p>OrCAD CIS (1)</p> <p>Allegro PCB Editor Intermediate Techniques (2)</p> <p>Allegro PCB Editor Basic Techniques (3)</p>	<p>Allegro Sigrity PI (1)</p> <p>Allegro Sigrity SI Foundations (2)</p> <p>PCB Design at RF - multi-Gigabit Transmission, EMI Control, and PCB Materials(2)</p> <p>Essential High-speed PCB Design for Signal Integrity(3)</p>	<p>Allegro PCB Librarian (2)</p> <p>Allegro Design Workbench for Librarians (2)</p>

▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). ^(NEW) New course (see online regional course catalog at cadence.com for a complete course listing).

Learning Map for IC Package Design and Analysis

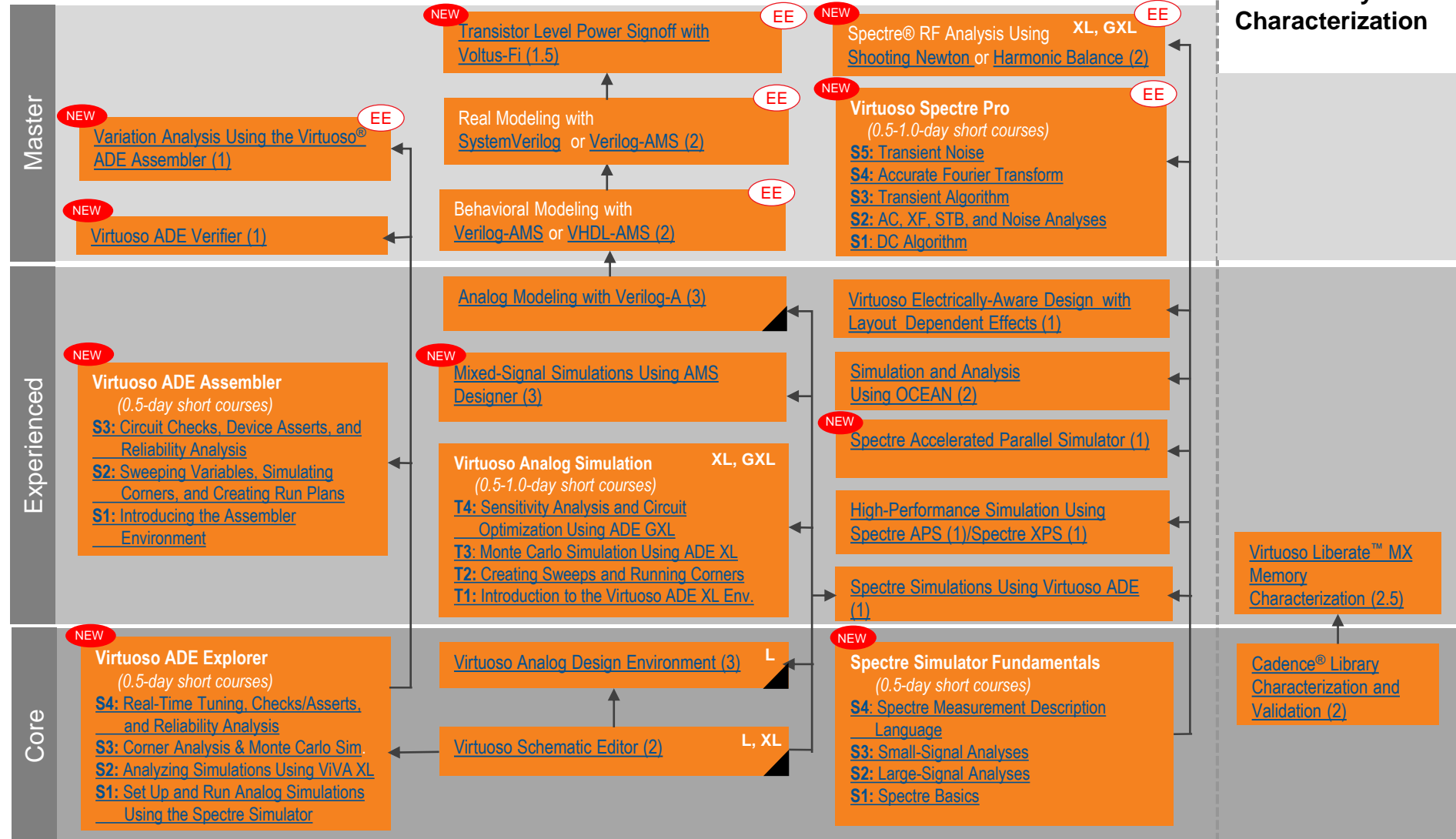
	SI/PI Analysis	IC Package Design
Analog Focus		
Master	<ul style="list-style-type: none"> Allegro® Sigrity™ System Serial Link Analysis (1) Sigrity PowerSI® for Model Generation and Analysis (2) 	
Experienced	<ul style="list-style-type: none"> Allegro Sigrity Power-Aware Parallel Bus Analysis (2) Sigrity PowerDC™ and OptimizePI™ (1) 	<ul style="list-style-type: none"> OrbitIO™ System Planner (1) Allegro Sigrity Package Assessment and Model Extraction (1)
	Allegro High-Speed Constraint Management (2)	
	Allegro Tool Setup and Configuration (2)	
Core	<ul style="list-style-type: none"> Allegro Sigrity PI (1) Allegro Sigrity SI Foundations (2) 	<ul style="list-style-type: none"> Allegro Package Designer (4) SiP Layout (5)

▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). **NEW** New course (see online regional course catalog at cadence.com for a complete course listing).

Learning Map for Custom Design with Virtuoso Technology – Custom IC, Analog and RF Design

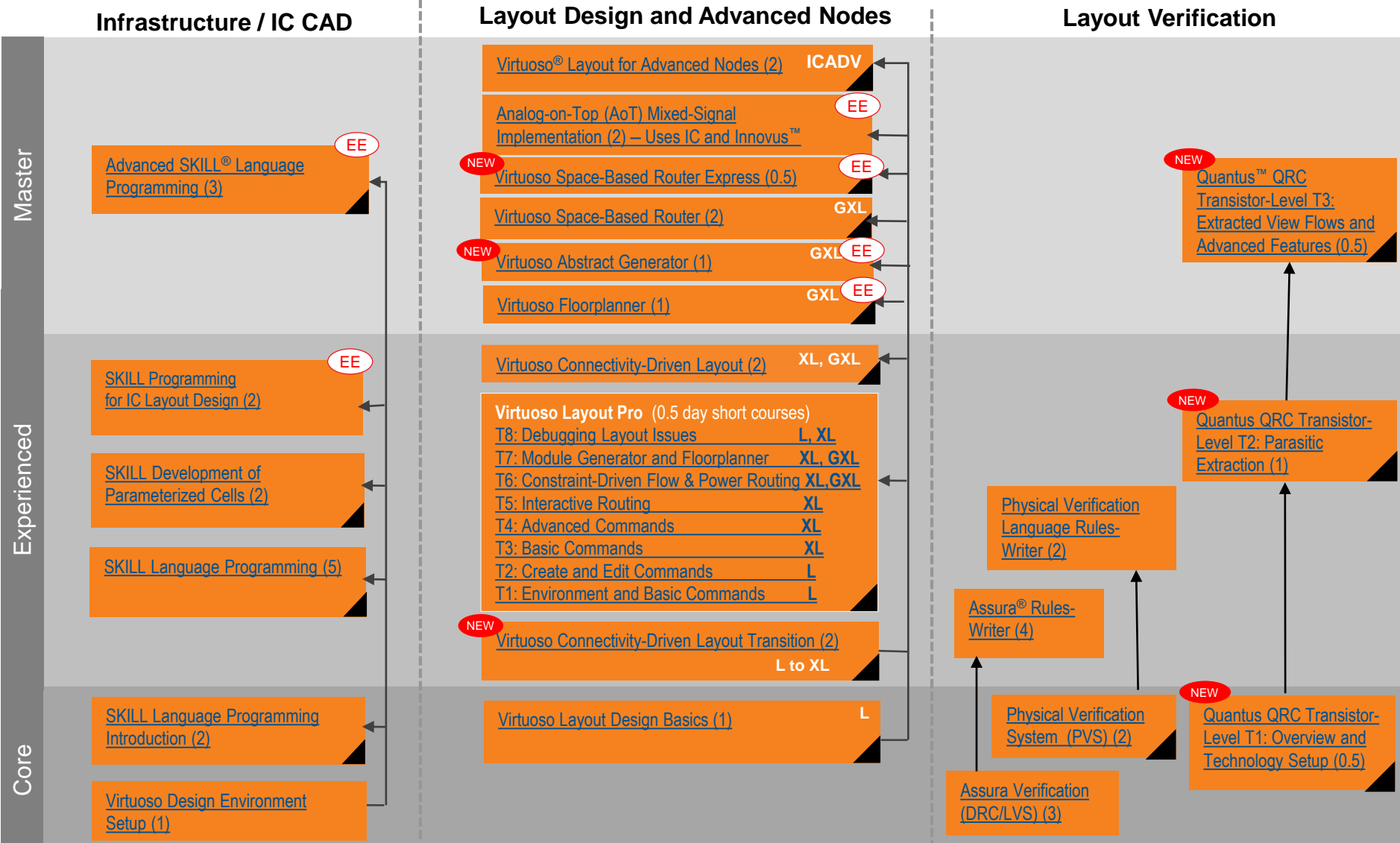
Circuit Design, Simulation, Modeling and RF Design

Library Characterization



▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). (NEW) New course (see online regional course catalog at cadence.com for a complete course listing).

Learning Map for Custom Design with Virtuoso Technology – Custom IC, Analog and RF Design



▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). (NEW) New course (see online regional course catalog at cadence.com for a complete course listing).

Learning Map for Digital Design and Signoff

Synthesis

Implementation

Silicon Signoff

Equivalence Checking

Master

NEW **GXL** **EE**
[Advanced Synthesis with Genus™ Synthesis Solution \(1\)](#)

Experienced

[Encounter® Test Jump Start to ATPG \(1\)](#)

XL
[Test Synthesis Using Encounter RTL Compiler \(1\)](#)

XL **EE**
[Low-Power Synthesis Flow with Genus Synthesis Solution \(1\)](#)

EE
[Fundamentals of IEEE 1801 Low-Power Specification Format \(1\)](#)

NEW **EE**
[Joules™ Power Calculator \(1\)](#)

Core

XL
[Genus Synthesis Solution \(2\)](#)

EE
[Analog-on-Top Mixed-Signal Implementation \(2\)](#)

EE
[Low-Power Flow with Innovus™ Implementation System \(1\)](#)

NEW
[Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis \(1\)](#)

[Innovus Implementation System \(Hierarchical\) \(1\)](#)

[Innovus Implementation System \(Block\) \(3\)](#)

[Virtuoso® Digital Implementation \(2\)](#)

XL **EE**
[Voltus™ Power-Grid Analysis and Signoff \(2\)](#)

XL
[Tempus™ Signoff Timing Analysis and Closure \(2\)](#)

[Basic Static Timing Analysis \(2\)](#)

XL
[Conformal® ECO \(1\)](#)

XL
[Low-Power Verification with Conformal \(1\)](#)

XL
[Logic Equivalence Checking with Conformal EC \(2\)](#)

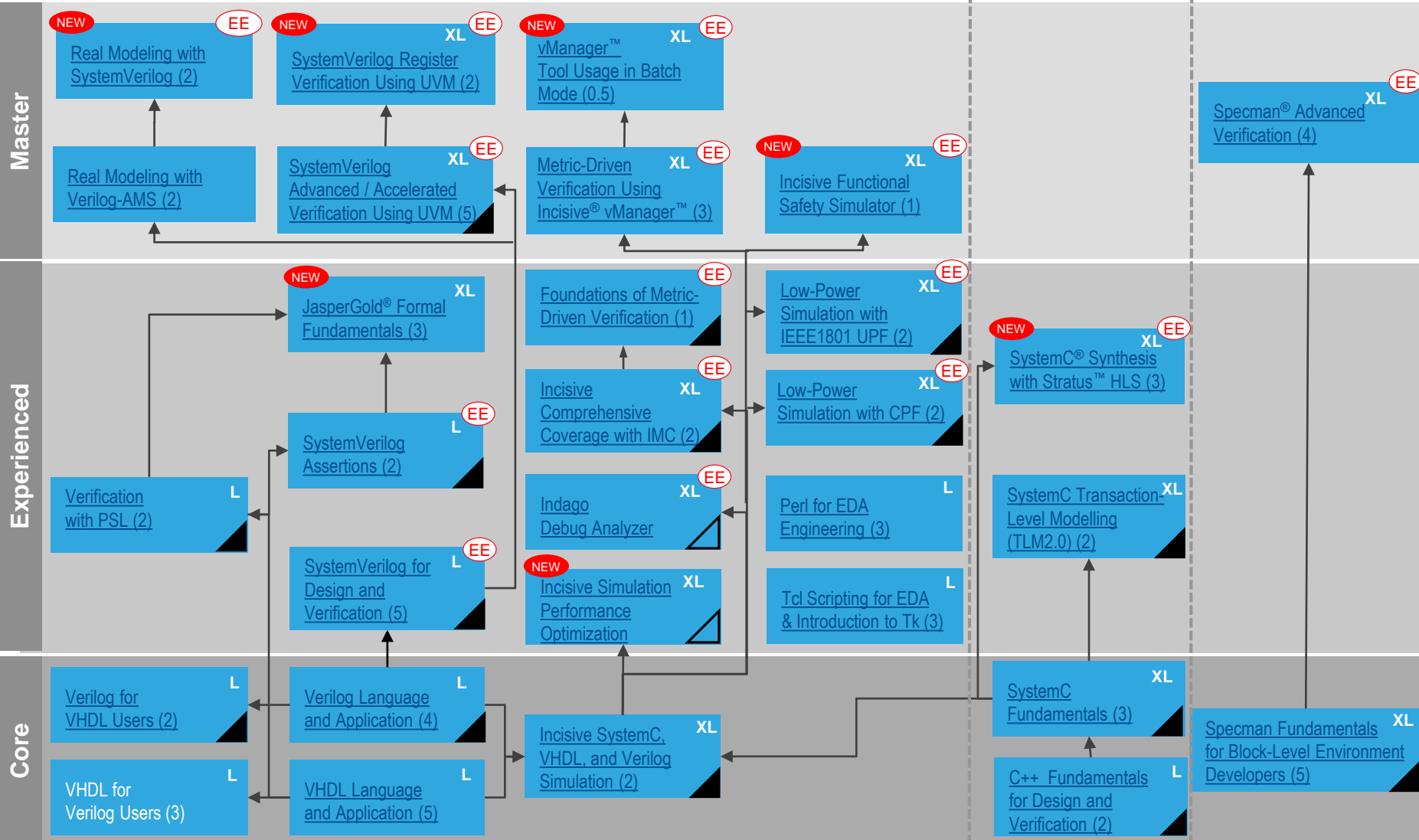
▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). **NEW** New course (see online regional course catalog at cadence.com for a complete course listing).

Learning Map for System Design and Verification – Languages, Methodologies, and Tools

HDL Design and Verification with Incisive

SystemC

Specman

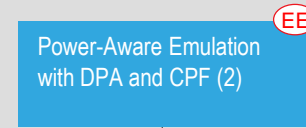
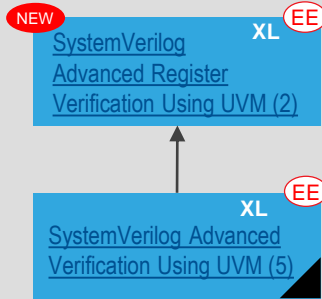


▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). (NEW) New course (see online regional course catalog at cadence.com for a complete course listing).

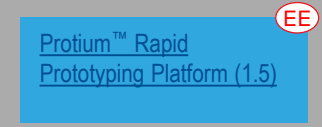
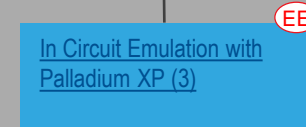
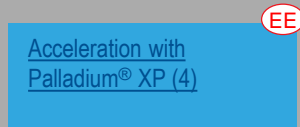
Acceleration

Emulation

Experienced

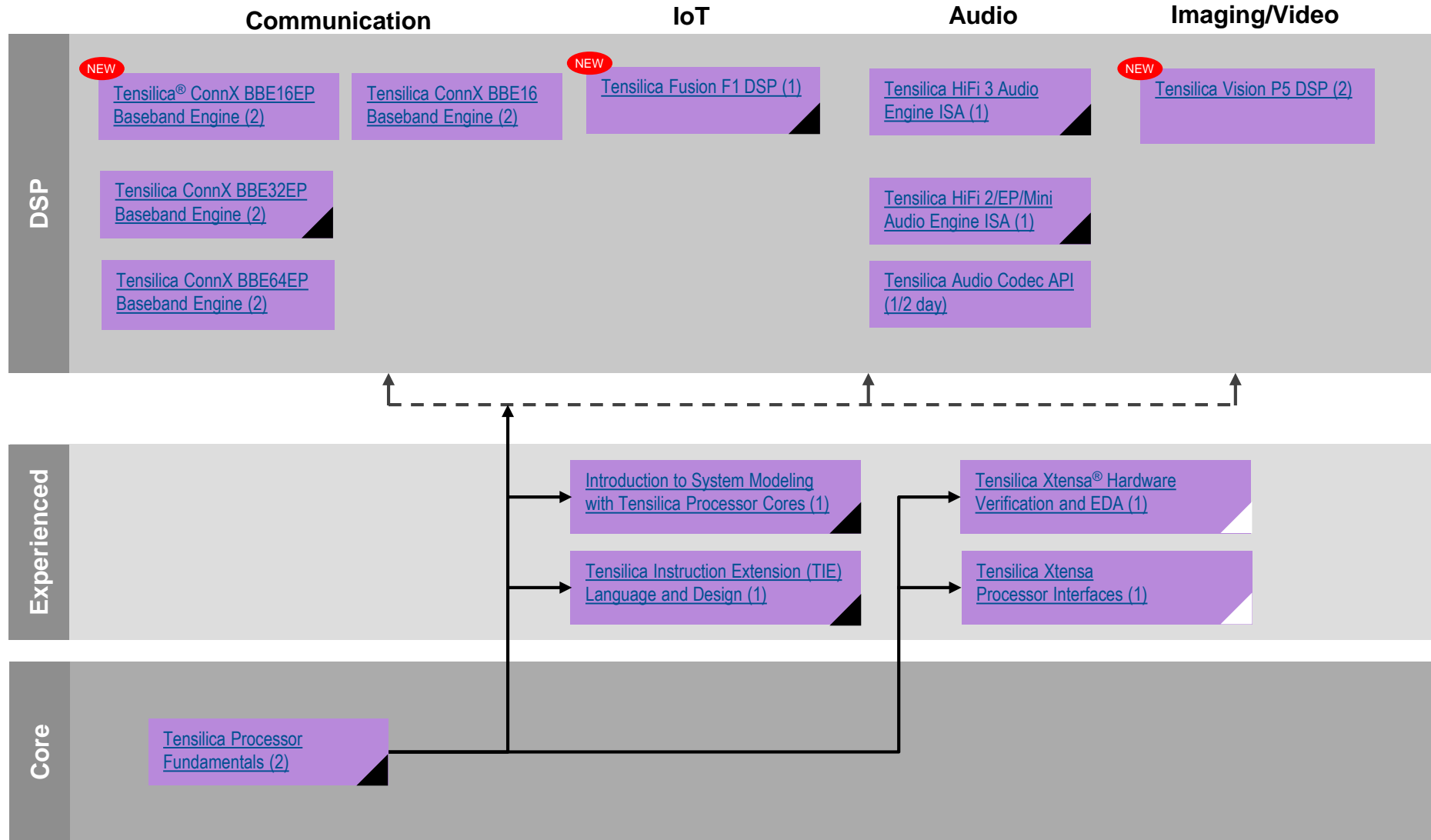


Core



▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). (NEW) New course (see online regional course catalog at cadence.com for a complete course listing).

Learning Map for Tensilica Processor IP



▲ Also available online. ▲ Online only. (EE) Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#). (NEW) New course (see online regional course catalog at cadence.com for a complete course listing).