Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents
• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
## IC Package Design and Analysis Learning Map

### IC Package Design
- **SiP Layout**
- **Allegro® Package Designer**
- **Allegro FPGA System Planner**
- **Allegro Sigrity Package Assessment and Model Extraction**
- **OrbitIO™ System Planner**
- **Advanced Design Verification with the RAVEL Programming Language**

### SI/PI Analysis
- **Allegro Sigrity™ SI Foundations**
- **Allegro Sigrity PI**
- **Sigity PowerDC™ and OptimizePI™**
- **Sigity SystemSI™ for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM**

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**New Course**

- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available

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Digital Design and Signoff Learning Map

### Synthesis and Test
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Synthesis Solution
  - Test Synthesis Using Genus Synthesis Solution
  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

### Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

### Silicon Signoff
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

### Equivalence Checking
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO

**Cadence® RTL-to-GDSII Flow**

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Simulation, Acceleration, Coverage and Debug

Incisive® SystemC®, VHDL, and Verilog Simulation

Incisive Simulation Performance Optimization

Perspec™ System Verifier - Basic

Low-Power Simulation with CPF

Low-Power Simulation with IEEE1801 UPF

Incisive Functional Safety Simulator

Xcelium™ Simulator

Cadence® RTL-To-GDSII Flow

Foundations of Metric-Driven Verification

Xcelium Integrated Coverage

Indago™ Debug Analyzer App

Metric-Driven Verification Using vManager™

vManager Tool Usage in Batch Mode

Specman® Fundamentals for Block-level Environment Developers

Specman Advanced Verification

VIP Basic Building Blocks and Usage

System Design and Verification Learning Map

New Course

Number of days for instructor-led course

Tiers of Cadence products used in course

Online Course Available

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