

Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

PCB Design and Analysis Learning Map

Beginner

































Advanced

Beginner





















Advanced

Logic Design

Allegro® Design Entry HDL Front-to-Back Flow   	Allegro Design Entry Using OrCAD® Capture  
Allegro Design Entry HDL Basics  	OrCAD CIS 
Allegro System Design Authoring   	Allegro EDM Design Entry HDL Front-to-Back Flow   
Allegro System Architect  	Allegro Team Design Authoring  
Allegro Design Reuse  	Allegro EDM for Engineers and Designers  
Allegro AMS Simulator  	Analog Simulation with PSpice®  
Allegro AMS Simulator Advanced Analysis  	Analog Simulation with PSpice Advanced Analysis  















PCB Design

Allegro PCB Editor Basic Techniques   
Allegro PCB Editor Intermediate Techniques  
Allegro PCB Router Basics  
Allegro PCB Editor Advanced Methodologies   
Allegro High-Speed Constraint Management   
Allegro Update Training   
Advanced Design Verification with the RAVEL Programming Language   

SI/PI Analysis

Essential High-Speed PCB Design for Signal Integrity 
PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials 
Allegro Sigrity™ SI Foundations  
Allegro Sigrity PI  
Sigrity PowerDC™ and OptimizePI™  
Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis  
Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM   

Library Development

Allegro PCB Librarian   
Allegro EDM PCB Librarian   
Allegro EDM for Administrators  
Allegro EDM Administration for OrCAD  
Allegro Design Entry HDL SKILL® Programming Language  
Allegro PCB Editor SKILL Programming Language  

IC Package Design and Analysis Learning Map

Beginner



Advanced

IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis **NEW**



Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM



Beginner



Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

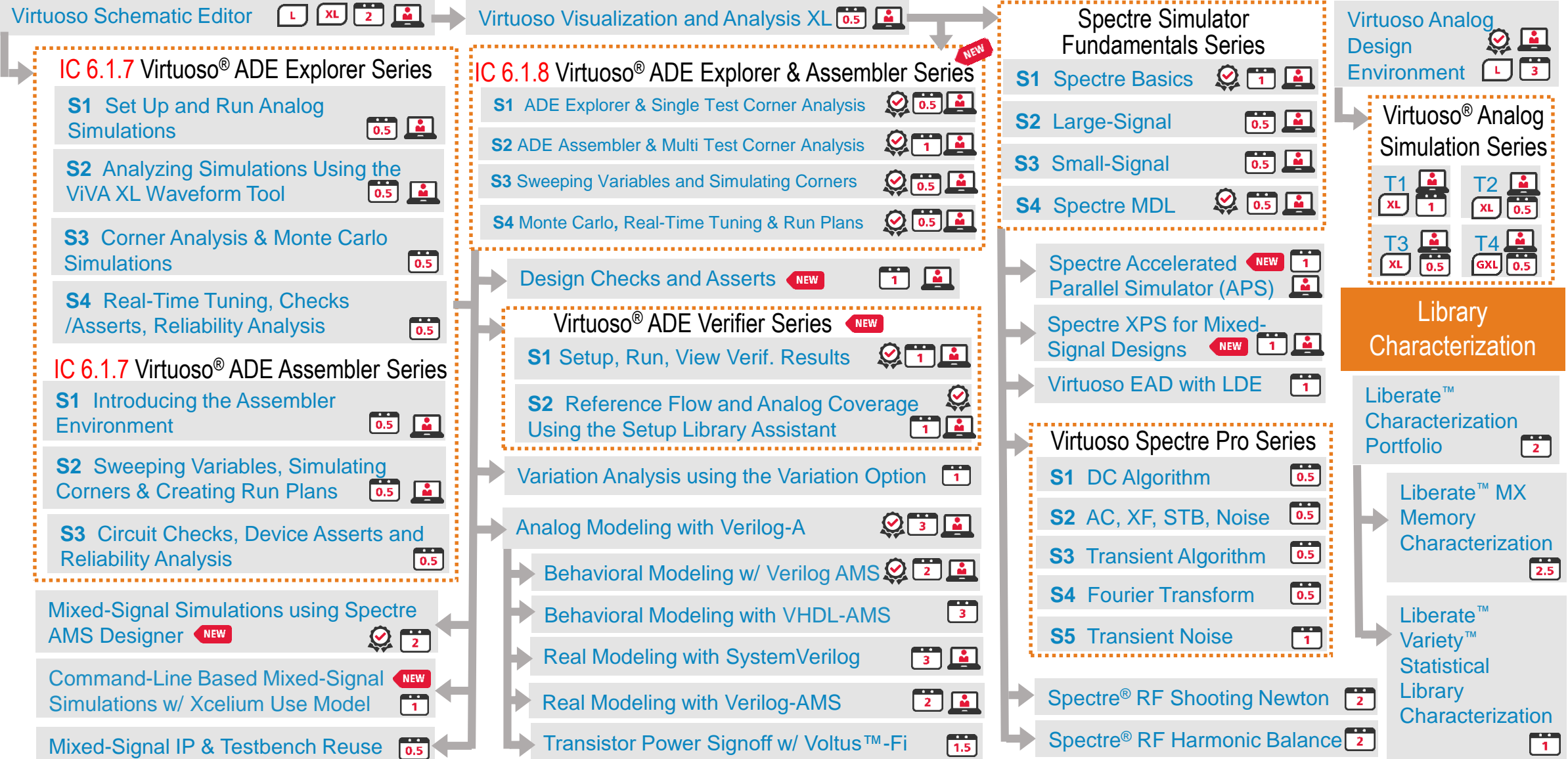
Beginner

Advanced

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design



Beginner

Advanced

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction
- SKILL Language Programming Fundamentals
- SKILL Language Programming
- SKILL Development of Parameterized Cells
- SKILL Programming for IC Layout Design
- Advanced SKILL Language Programming

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics
- Virtuoso Connectivity-Driven Layout Transition
- Virtuoso Abstract Generator
- Virtuoso Floorplanner
- Virtuoso Space-Based Router
- Virtuoso Space-Based Router Express
- Virtuoso® Advanced-Node Series – ICADV
 - Virtuoso Layout for Advanced Nodes
 - T1: Place and Route
 - T2: Electromigration
- Virtuoso® Layout Pro Series
 - T1: Env. and Basic Commands
 - T2: Create and Edit Commands
 - T3: Basic Commands
 - T4: Advanced Commands
 - T5: Interactive Routing
 - T6: Constraint-Driven Flow and Power Routing
 - T7: Module Generator and Floorplanner
 - T8: Debugging Layout Issues

Layout Verification

- Physical Verification System (PVS)
- Physical Verification Language Rules-Writer
- Quantus™ Extraction Solution Transistor-Level Series
- T1: Overview and Technology Setup
- T2: Parasitic Extraction
- T3: Extracted View Flows and Advanced Features

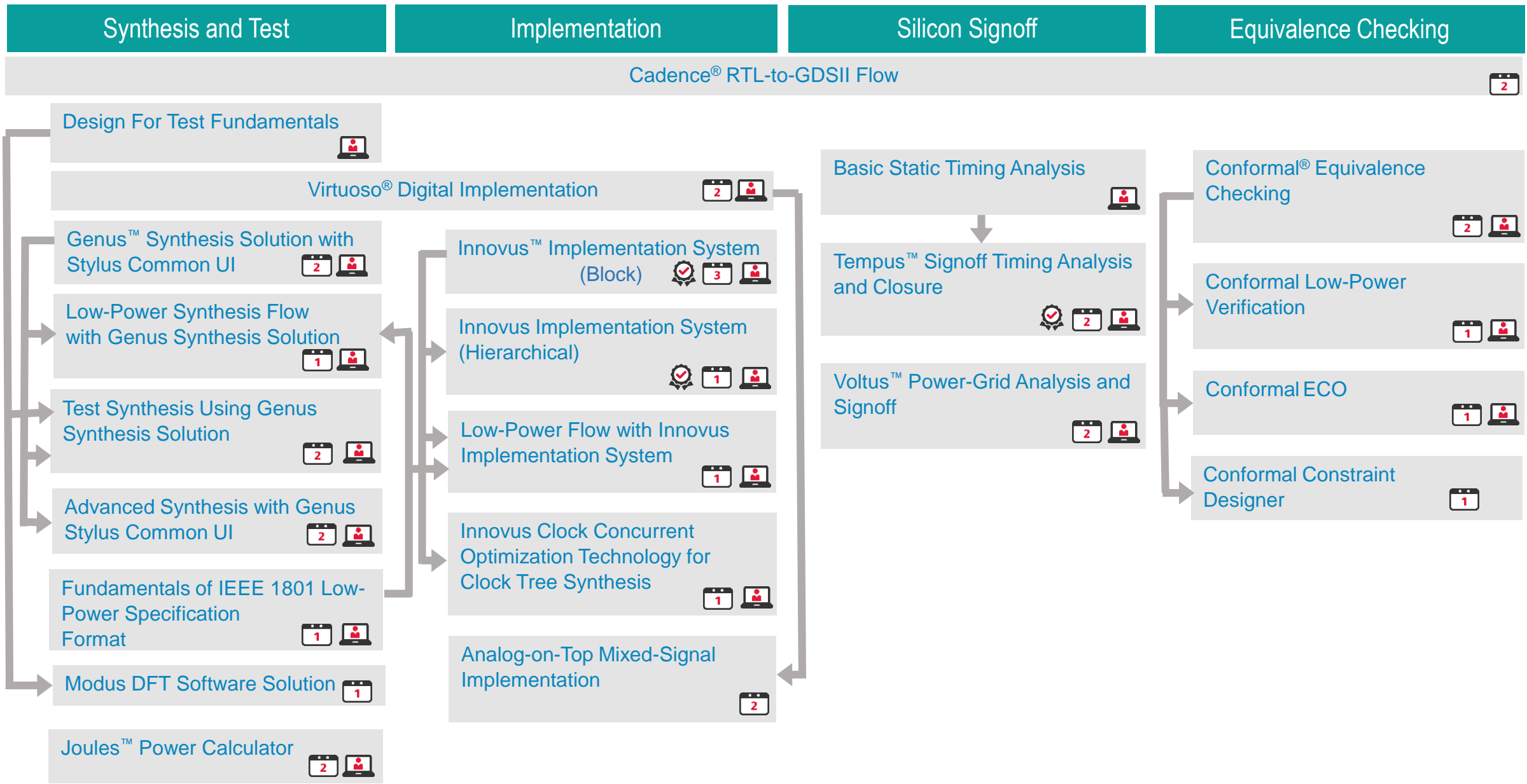
Digital Design and Signoff Learning Map

Beginner

Advanced

Beginner

Advanced



System Design and Verification Learning Map

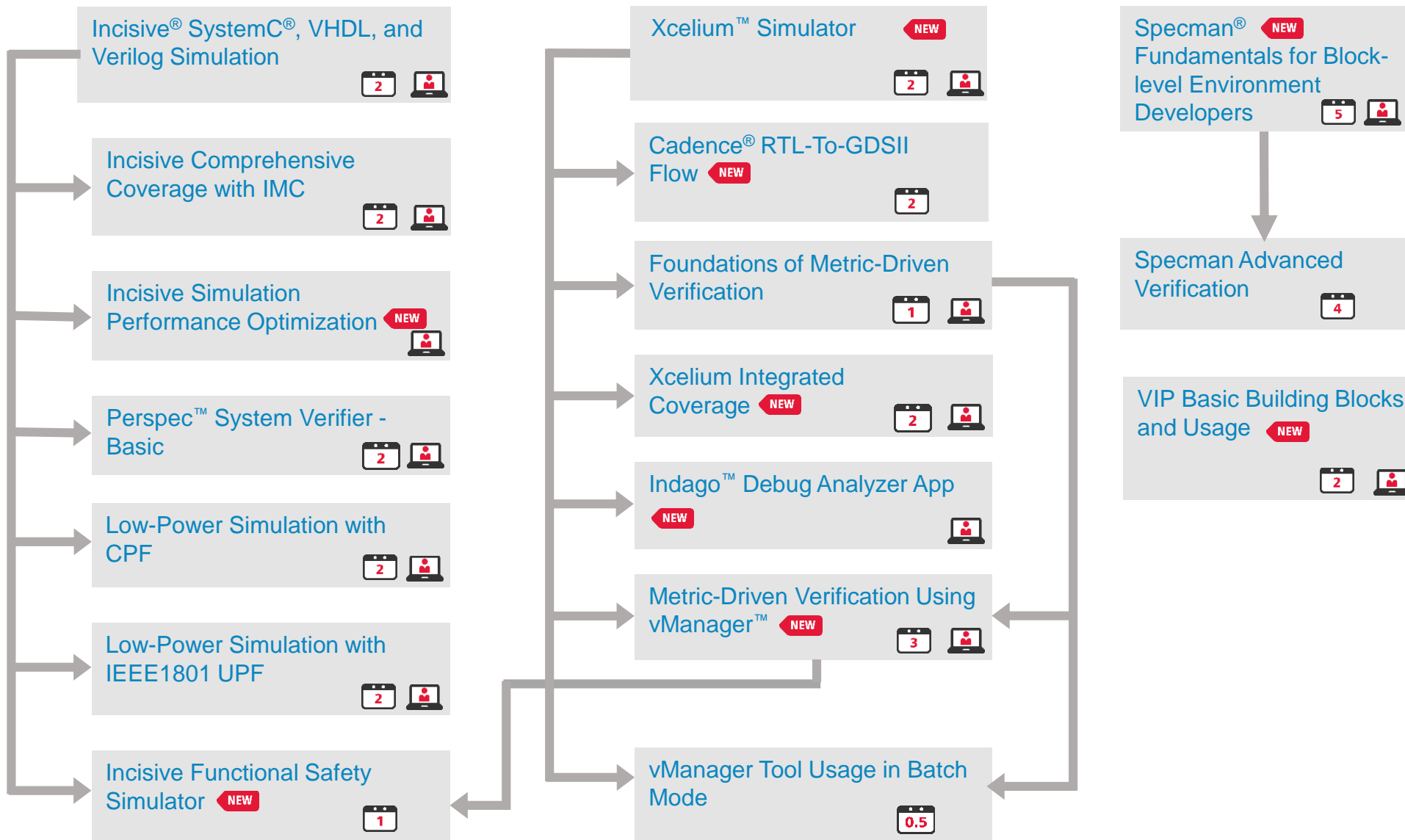
Beginner

Advanced

Beginner

Advanced

Simulation, Acceleration, Coverage and Debug



System Design and Verification Learning Map

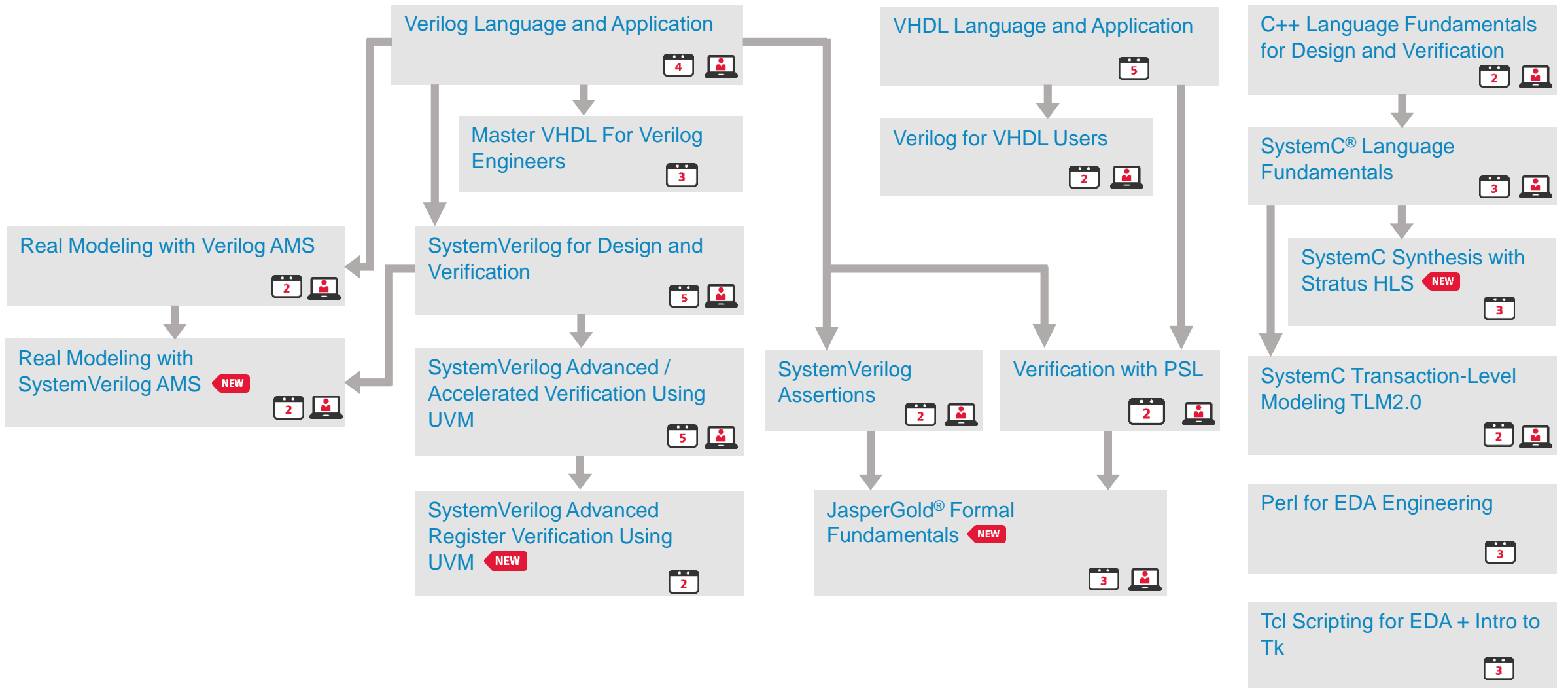
Beginner

Advanced

Beginner

Advanced

Design and Verification Languages



Tensilica Processor IP Learning Map

Tensilica Processors

ConnX DSP

Fusion DSP

HiFi Audio DSP

Vision DSP

Tensilica® Processor Fundamentals



Tensilica Xtensa® Processor Interfaces



Tensilica Xtensa Hardware Verification and EDA



Tensilica Instruction Extension Language and Design



Introduction to System Modeling with Tensilica Processor Cores



Tensilica ConnX BBE16EP Baseband Engine



Tensilica ConnX BBE32EP Baseband Engine



Tensilica ConnX BBE64EP Baseband Engine



Tensilica Fusion F1 DSP



Tensilica Fusion G3 DSP



Tensilica Fusion G6 DSP



Tensilica Audio Codec API



Tensilica HiFi 2/EP/Mini Audio Engine ISA



Tensilica HiFi 3 Audio Engine ISA



Tensilica HiFi 4 DSP **NEW**



Tensilica Vision P5 DSP



Tensilica Vision P6 DSP



Tensilica Vision C5 DSP **NEW**



New Course



Number of days for instructor-led course



Online Course Available

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