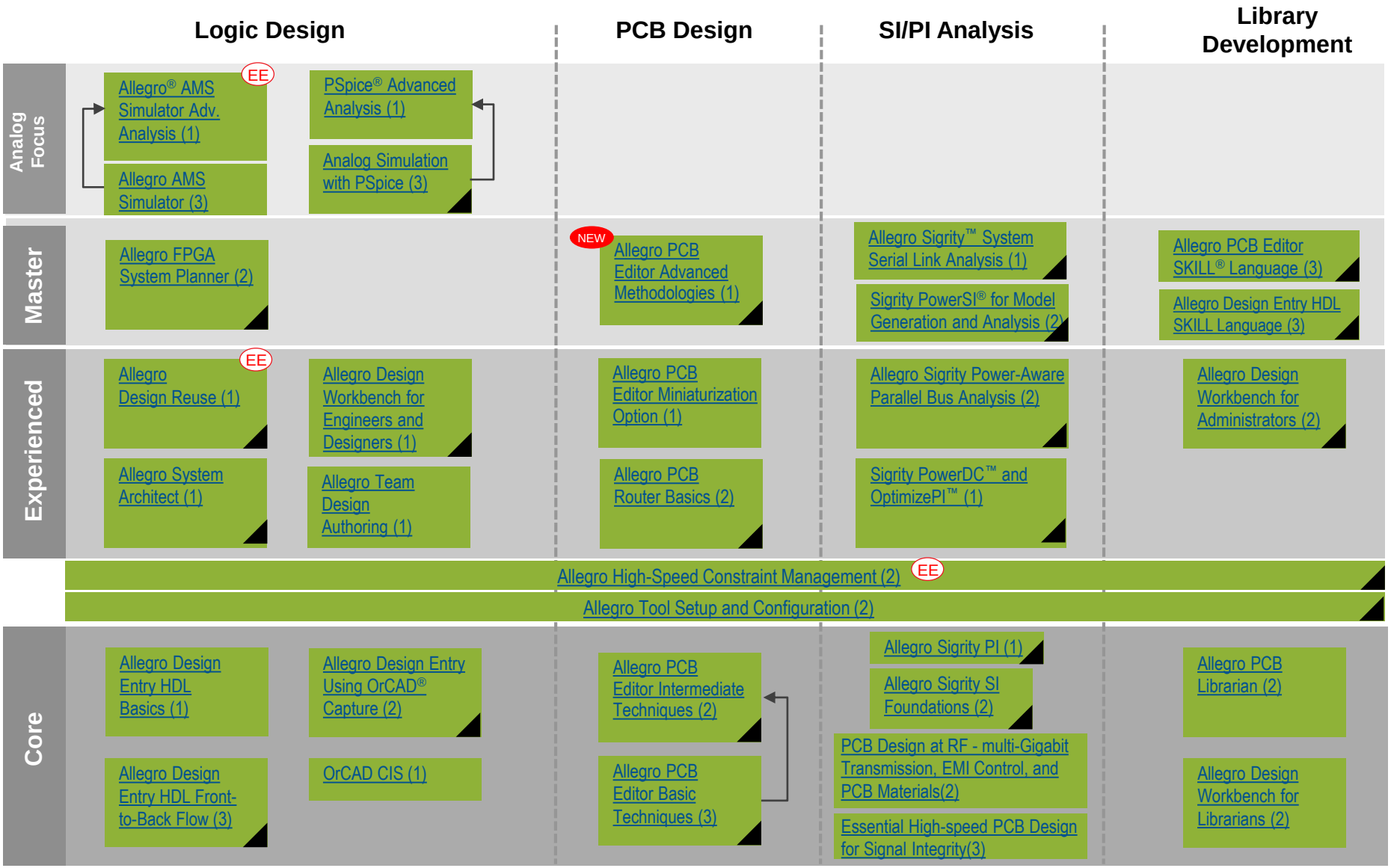
Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

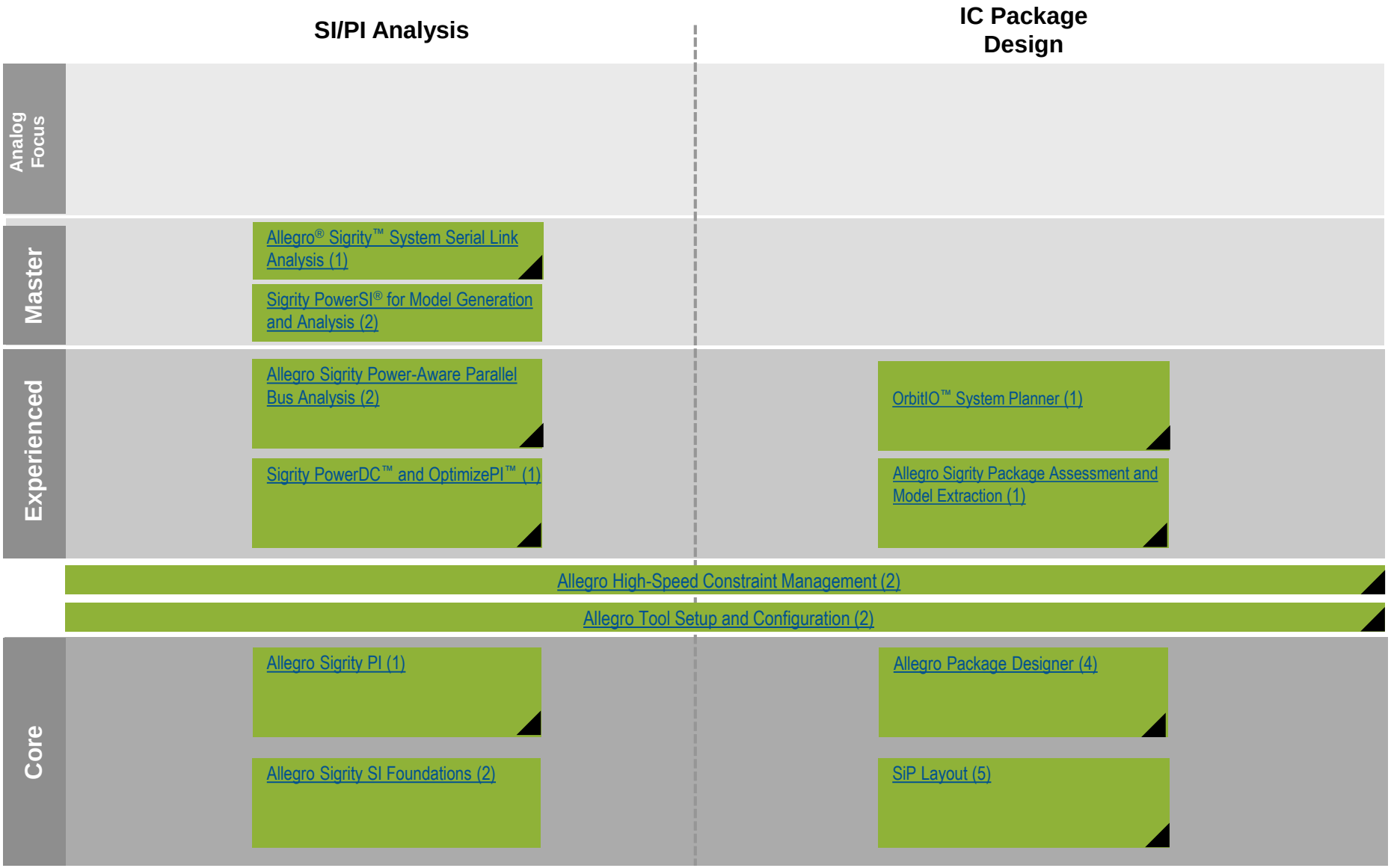
Learning Map for PCB Design and Analysis



◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for IC Package Design and Analysis



◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for
Custom Design with Virtuoso Technology – *Custom IC, Analog and RF Design*

1 of 2 – see next page

Circuit Design, Simulation, Modeling and RF Design

Library Characterization

Master

NEW EE Transistor Level Power Signoff with Voltus-Fi (1.5)

NEW EE Spectre® RF Analysis Using Shooting Newton or Harmonic Balance (2) — XL, GXL

EE Real Modeling with SystemVerilog or Verilog-AMS (2)

NEW EE **Virtuoso Spectre Pro** *(0.5-1.0-day short courses)*
- **S5:** Transient Noise
- **S4:** Accurate Fourier Transform
- **S3:** Transient Algorithm
- **S2:** AC, XF, STB, and Noise Analyses
- **S1:** DC Algorithm

NEW EE Variation Analysis Using the Virtuoso® ADE Assembler (1)

EE Behavioral Modeling with Verilog-AMS or VHDL-AMS (2)

NEW Virtuoso ADE Verifier (1)

Experienced

Analog Modeling with Verilog-A (3)

Virtuoso Electrically-Aware Design with Layout Dependent Effects (1)

NEW **Virtuoso ADE Assembler** *(0.5-day short courses)*
- **S3:** Circuit Checks, Device Asserts, and Reliability Analysis
- **S2:** Sweeping Variables, Simulating Corners, and Creating Run Plans
- **S1:** Introducing the Assembler Environment

NEW Mixed-Signal Simulations Using AMS Designer (3)

Simulation and Analysis Using OCEAN (2)

NEW Spectre Accelerated Parallel Simulator (1)

Virtuoso Analog Simulation — XL, GXL *(0.5-1.0-day short courses)*
- **T4:** Sensitivity Analysis and Circuit Optimization Using ADE GXL
- **T3:** Monte Carlo Simulation Using ADE XL
- **T2:** Creating Sweeps and Running Corners
- **T1:** Introduction to the Virtuoso ADE XL Env.

High-Performance Simulation Using Spectre APS (1)/Spectre XPS (1)

Virtuoso Liberate™ MX Memory Characterization (2.5)

Spectre Simulations Using Virtuoso ADE (1)

Core

NEW **Virtuoso ADE Explorer** *(0.5-day short courses)*
- **S4:** Real-Time Tuning, Checks/Asserts, and Reliability Analysis
- **S3:** Corner Analysis & Monte Carlo Sim.
- **S2:** Analyzing Simulations Using ViVA XL
- **S1:** Set Up and Run Analog Simulations Using the Spectre Simulator

Virtuoso Analog Design Environment (3) — L

Virtuoso Schematic Editor (2) — L, XL

NEW **Spectre Simulator Fundamentals** *(0.5-day short courses)*
- **S4:** Spectre Measurement Description Language
- **S3:** Small-Signal Analyses
- **S2:** Large-Signal Analyses
- **S1:** Spectre Basics

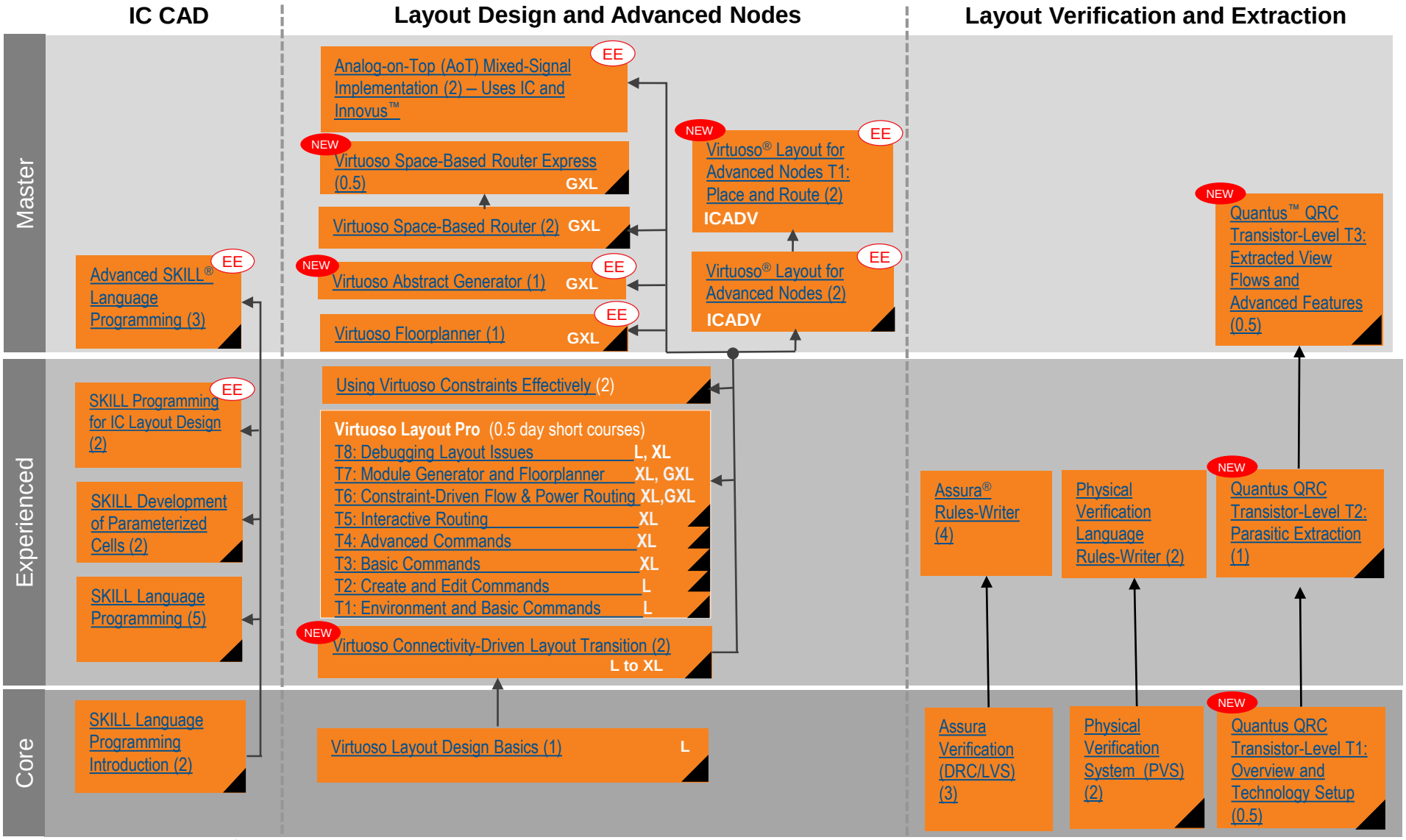
Cadence® Library Characterization and Validation (2)

◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for
Custom Design with Virtuoso Technology – *Custom IC, Analog and RF Design*

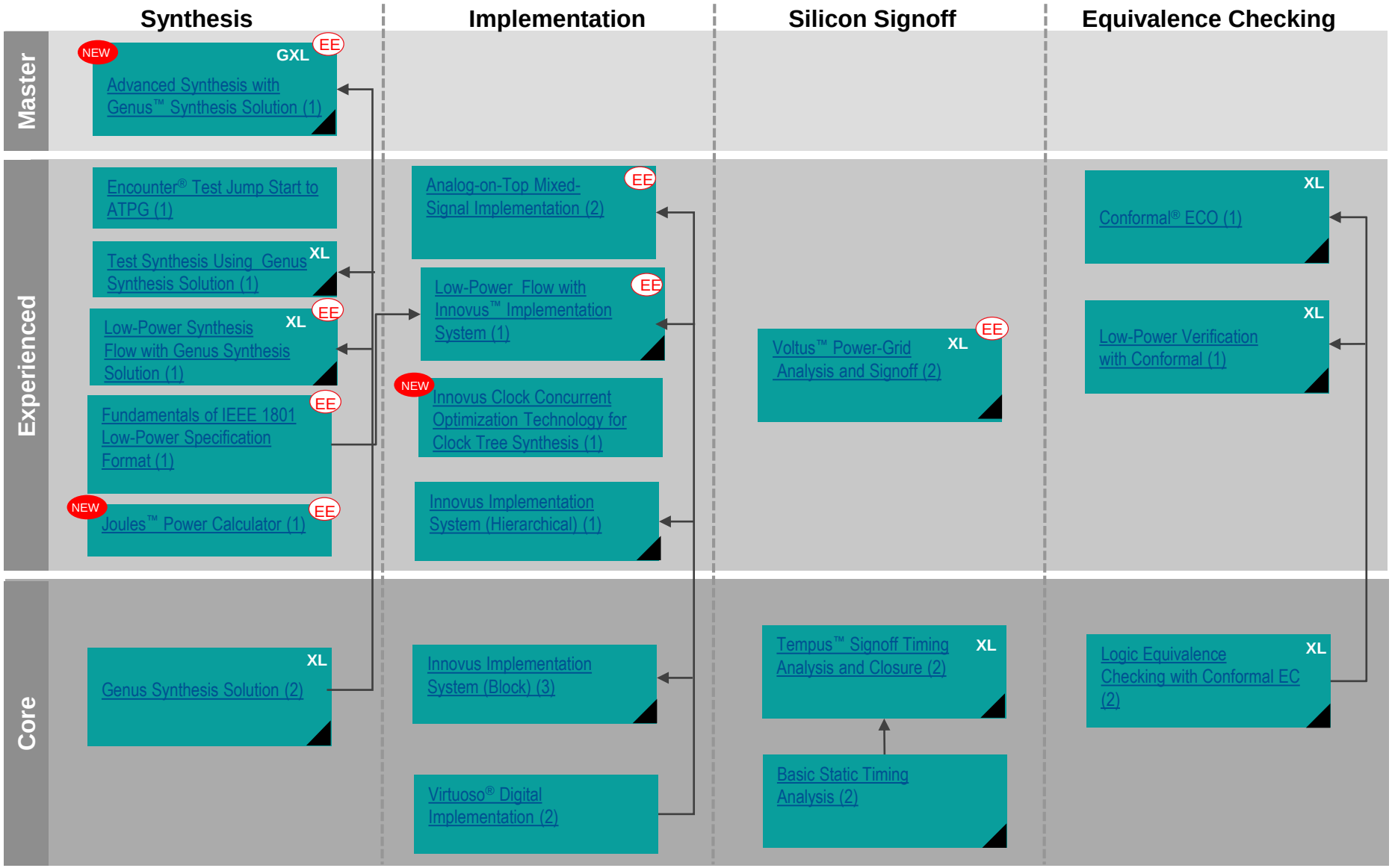
2 of 2 – see prior page



◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for Digital Design and Signoff

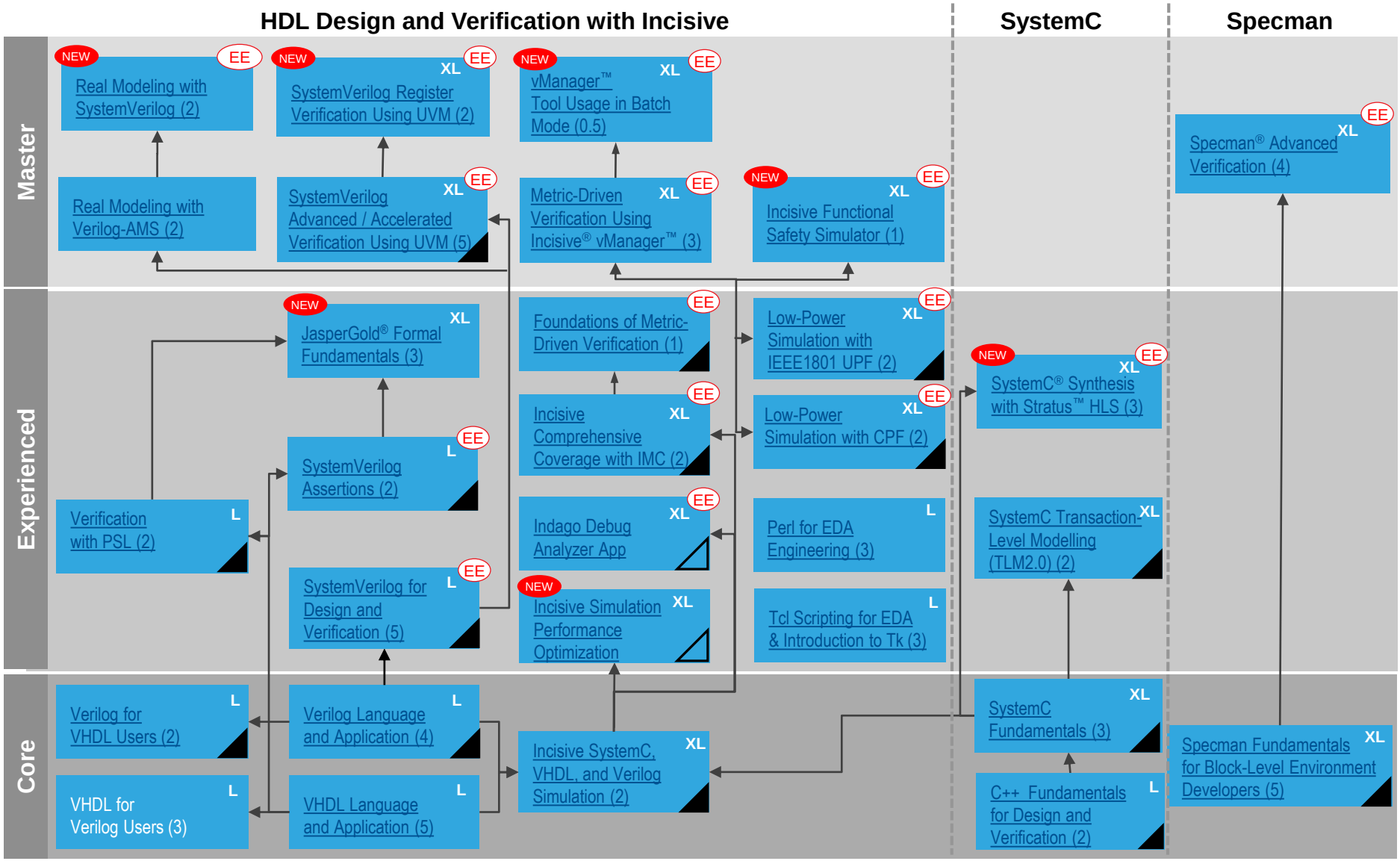


◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for System Design and Verification – Languages, Methodologies, and Tools

1 of 2 – see next page

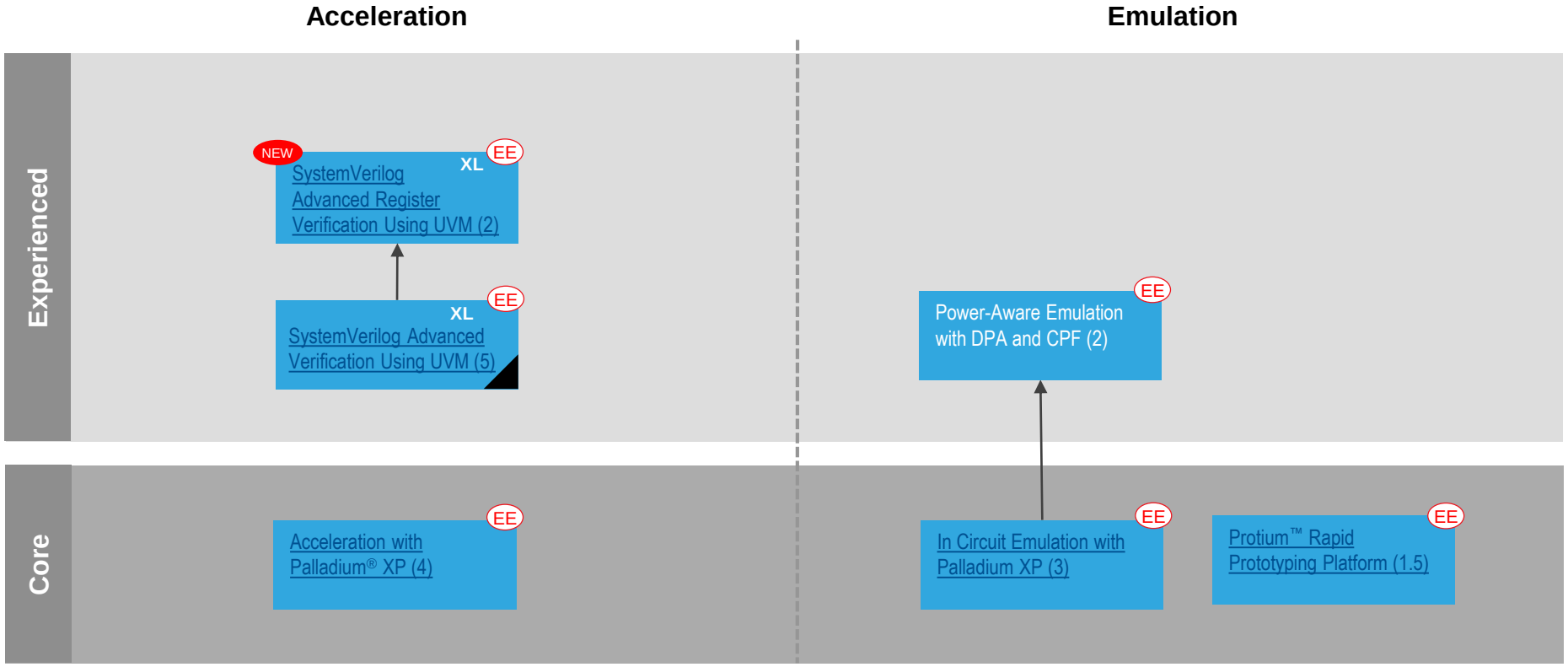


◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for System Design and Verification – Acceleration and Emulation

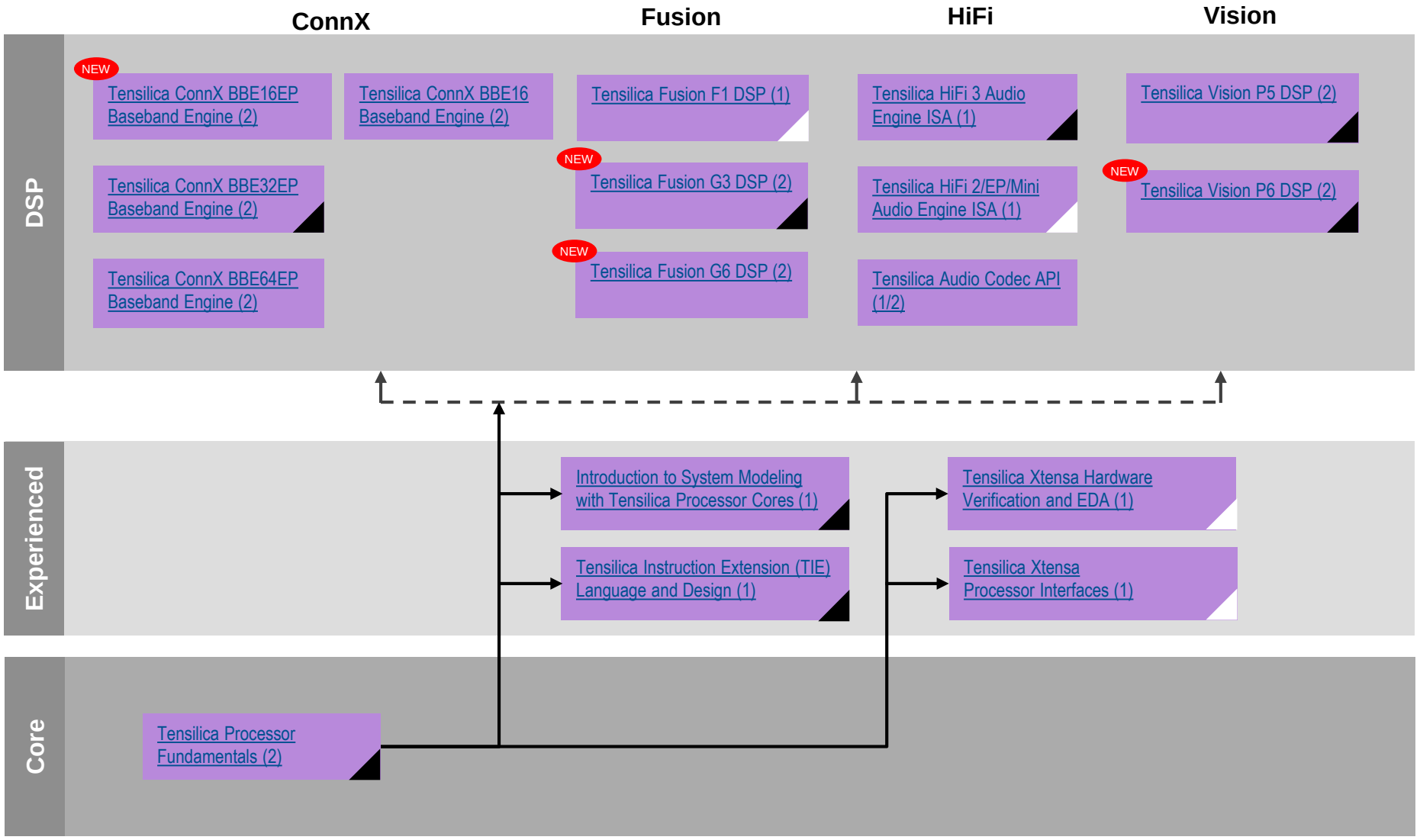
2 of 2 – see prior page



◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0

Learning Map for Tensilica Processor IP



◢ Also available online. ◿ Online only. (EE) Denotes Advance with Engineer Explorer course. **L, XL, GXL** denotes tiers of Cadence® products used in course (not applicable if no legend). (#) Denotes number of days for instructor-led training**.** Several self-paced courses are only available in our **Online Training Collection**. NEW New course (see course catalog at cadence.com for a complete course listing).

V14.0