Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
## IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Number of Days</th>
<th>Tiers of Cadence Products Used in Course</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

## SI/PI Analysis

<table>
<thead>
<tr>
<th>Course</th>
<th>Number of Days</th>
<th>Tiers of Cadence Products Used in Course</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allegro Sigrity™ SI Foundations</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Allegro Sigrity PI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sigtry PowerDC™ and OptimizePI™</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Sigtry SystemSI™ for Parallel Bus and Serial Link Analysis</td>
<td>NEW</td>
<td></td>
</tr>
<tr>
<td>Sigtry PowerSI® for Model Generation and Analysis</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>
Custom IC, Analog and RF Design Learning Map

Virtuoso® Analog Design Environment

Virtuoso Analog Simulation Series

**T1** The Virtuoso Analog Design XL Environment

**T2** Creating Sweeps and Running Corner Analysis

**T3** Monte Carlo Simulation Using ADE XL

**T4** Sensitivity Analysis and Circuit Optimization Using ADE GXL

Mixed-Signal Simulations using Spectre MDL

Analog Modeling with Verilog-A

Behavioral Modeling with / Verilog-AMS / VHDL-AMS

Real Modeling with / SystemVerilog / Verilog-AMS

Transistor-Level Power Signoff with Voltus™-Fi

Virtuoso ADE Explorer Series

**S1** Set Up and Run Analog Simulations Using the Spectre® Simulator

**S2** Analyzing Simulations Using the VIVA XL Waveform Tool

**S3** Corner Analysis and Monte Carlo Simulations

**S4** Real-Time Tuning, Checks/Asserts, and Reliability Analysis

Virtuoso ADE Assembler Series

**S1** Introducing the Assembler Environment

**S2** Sweeping Variables, Simulating Corners and Creating Run Plans

**S3** Circuit Checks, Device Asserts and Reliability Analysis

Virtuoso ADE Verifier

Variation Analysis Using the Virtuoso Variation Option

Spectre Simulator Fundamentals Series

**S1** Spectre Basics

**S2** Large-Signal

**S3** Small-Signal

**S4** Spectre MDL Design Checks & Asserts

Virtuoso EAD with LDE

Spectre Accelerated Parallel Simulator (APS)

Spectre XPS for Mixed-Signal Designs

Virtuoso Spectre Pro Series

**S1** DC Algorithm

**S2** AC, XF, STB, Noise

**S3** Transient Algorithm

**S4** Fourier Transform

**S5** Transient Noise

Spectre® RF/ Shooting Newton / Harmonic Balance

Library Characterization

Cadence® Library Characterization and Validation

Virtuoso Liberate™ MX for Memory Characterization

Cadence Variety™ Statistical Library Characterization

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Online Course Available
Digital Design and Signoff Learning Map

**Synthesis**
- Genus™ Synthesis Solution
- Low-Power Synthesis Flow with Genus Synthesis Solution
- Test Synthesis Using Genus Synthesis Solution
- Advanced Synthesis with Genus Synthesis Solution
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

**Implementation**
- Virtuoso® Digital Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO
- Conformal Constraint Designer

**Notes:**
- New Course
- Number of days for instructor-led course
- Online Course Available

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