Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
## PCB Design and Analysis Learning Map

### Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
- **Allegro Design Entry Using OrCAD® Capture**
- **OrCAD CIS**
- **OrCAD Capture Constraint Manager PCB Flow**
- **Allegro System Capture**
- **Allegro System Architect**
- **Allegro Design Reuse**
- **Allegro AMS Simulator**
- **Allegro AMS Simulator Advanced Analysis**

### PCB Design
- **Allegro PCB Editor Basic Techniques**
- **Allegro PCB Editor Intermediate Techniques**
- **Allegro PCB Router Basics**
- **Allegro PCB Editor Advanced Methodologies**
- **Allegro High-Speed Constraint Management**
- **Advanced Design Verification with the RAVEL Programming Language**

### SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
- **Allegro Sigtry™ SI Foundations**
- **Allegro Sigtry PI**
- **Sigrity PowerDC™ and OptimizePI™**
- **Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**
- **Clarity 3D Solver**
- **Celsius Thermal**

### Library Development
- **Allegro PCB Librarian**
- **Allegro EDM for Administrators**
- **Allegro Design Entry HDL SKILL® Programming Language**
- **Allegro PCB Editor SKILL Programming Language**
## IC Package Design and Analysis Learning Map

### IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Tiers</th>
<th>Days</th>
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<tbody>
<tr>
<td>SiP Layout</td>
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<tr>
<td>Allegro® Package Designer</td>
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<tr>
<td>Allegro FPGA System Planner</td>
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<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
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<tr>
<td>OrbitIO™ System Planner</td>
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<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
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<tr>
<td>Allegro Package Designer Plus</td>
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### SI/PI Analysis

<table>
<thead>
<tr>
<th>Course</th>
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<th>Days</th>
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<tr>
<td>Allegro Sigrity™ SI Foundations</td>
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<tr>
<td>Allegro Sigrity PI</td>
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<td>Sigtry PowerDC™ and OptimizePI™</td>
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<tr>
<td>Sigtry SystemSI™ for Parallel Bus and Serial Link Analysis</td>
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<tr>
<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
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</table>
Custom IC, Analog and RF Design Learning Map

Circuit Design, Simulation, Modeling and RF Design

**Analog Modeling with Verilog-A**
- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model
- Behavioral Modeling with Verilog AMS
- Behavioral Modeling with VHDL-AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

**Virtuoso Schematic Editor**

**Virtuoso Visualization and Analysis**

**Virtuoso® ADE Explorer & Assembler Series**
- S1 ADE Explorer & Single Test Corner Analysis
- S2 ADE Assembler & Multi Test Corner Analysis
- S3 Sweeping Variables and Simulating Corners
- S4 Monte Carlo, Real-Time Tuning & Run Plans

**Virtuoso® ADE Verifier Series**
- S1 Setup, Run, View Verif. Results
- S2 Reference Flow and Analog Coverage Using the Setup Library Assistant

**Design Checks and Asserts**

**Spectre® Simulator Fundamentals Series**
- S1 Spectre Basics
- S2 Large-Signal
- S3 Small-Signal
- S4 Spectre MDL

**Spectre Accelerated Parallel Simulator (APS)**

**Spectre XPS for Mixed-Signal Designs**

**Virtuoso® Spectre® Pro Series**
- S1 DC Algorithm
- S2 AC, XF, STB, Noise
- S3 Transient Algorithm
- S4 Fourier Transform
- S5 Transient Noise

**Spectre® RF Shooting Newton**

**Spectre® RF Harmonic Balance**
### Custom IC, Analog and RF Design Learning Map

#### IC CAD
- **SKILL® Language Programming Introduction**
- **SKILL Language Programming**
- **SKILL Development of Parameterized Cells**
- **SKILL Programming for IC Layout Design**
- **Advanced SKILL Language Programming**

#### Layout Design and Advanced Nodes
- **Virtuoso® Layout Design Basics**
- **Virtuoso Connectivity-Driven Layout Transition**
- **Virtuoso Abstract Generator**
- **Virtuoso Floorplanner**
- **Virtuoso Space-Based Router**
- **Virtuoso Advanced-Node – ICADV**
- **Virtuoso Layout for Adv. Nodes**
- **T1: Place and Route**
- **T2: Electromigration**

#### Virtuoso® Layout Pro Series
- **T1: Env. and Basic Commands**
- **T2: Create and Edit Commands**
- **T3: Basic Commands**
- **T4: Advanced Commands**
- **T5: Interactive Routing**
- **T6: Constraint-Driven Flow and Power Routing**
- **T7: Module Generator and Floorplanner**
- **T8: Debugging Layout Issues**
- **T9: Virtuoso Design Planner**

#### Virtuoso® Advanced-Node and Methodology Platform – ICADVM
- **Virtuoso Layout for Advanced Nodes and Methodology Platform**

#### Layout Verification
- **Quantus™ Extraction Solution Transistor-Level Series**
- **T1: Overview and Technology Setup**
- **T2: Parasitic Extraction**
- **T3: Extracted View Flows and Advanced Features**
- **Physical Verification System (PVS)**
- **Physical Verification Language Rules-Writer**
- **Transistor Level Power Signoff with Voltus™-Fi**

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**New Course**

**Number of days for instructor-led course**

**Tiers of Cadence products used in course**

**Online Course Available**

**Digital Badge Available**
System Design and Verification Learning Map

Simulation, Coverage and Debug

Xcelium™ Simulator

- Cadence® RTL-To-GDSII Flow
  
- VIP Basic Building Blocks and Usage
  
- Low-Power Simulation with CPF
  
- Low-Power Simulation with IEEE1801 UPF

- Foundations of Metric-Driven Verification
  
- Xcelium Integrated Coverage
  
- Metric-Driven Verification Using vManager™
  
- vManager Tool Usage in Batch Mode

- Specman® Fundamentals for Block-Level Environment Developers
  
- Indago™ Debug Analyzer App
  
- Perspec System Verifier - Basic
  
- Incisive Functional Safety Simulator
  
- Specman Advanced Verification