Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

PCB Design and Analysis Learning Map

Beginner

Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow
- Allegro Design Entry HDL Basics
- Allegro System Design Authoring NEW
- Allegro System Architect
- Allegro Design Reuse
- Allegro AMS Simulator
  - Allegro AMS Simulator Advanced Analysis
- Allegro Design Entry Using OrCAD® Capture
- OrCAD CIS
- Allegro EDM Design Entry HDL Front-to-Back Flow NEW
- Allegro Team Design Authoring
- Allegro EDM for Engineers and Designers
- Analog Simulation with PSpice®
  - Analog Simulation with PSpice Advanced Analysis

PCB Design

- Allegro PCB Editor Basic Techniques
  - Allegro PCB Editor Intermediate Techniques
  - Allegro PCB Router Basics
  - Allegro PCB Editor Advanced Methodologies NEW
- Allegro High-Speed Constraint Management
- Allegro Update Training NEW
- Advanced Design Verification with the RAVEL Programming Language NEW

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
- Allegro Sigrity™ SI Foundations
- Allegro Sigrity PI
- Sigrity PowerDC™ and OptimizePI™
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM NEW

Library Development

- Allegro PCB Librarian
- Allegro EDM PCB Librarian NEW
- Allegro EDM for Administrators
- Allegro EDM Administration for OrCAD
- Allegro Design Entry HDL SKILL® Programming Language
- Allegro PCB Editor SKILL Programming Language

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout — 4 days, online
- Allegro® Package Designer — 4 days, online
- Allegro FPGA System Planner — 2 days, online
- Allegro Sigrity Package Assessment and Model Extraction — 1 day, online
- OrbitIO™ System Planner — 1 day, online
- Advanced Design Verification with the RAVEL Programming Language NEW — 2 days, online

SI/PI Analysis

- Allegro Sigrity™ SI Foundations — 2 days, online
- Allegro Sigrity PI — 1 day, online
- Sigrity PowerDC™ and OptimizePI™ — 1 day, online
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis NEW — 3 days, online
- Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM — 2 days, online

Beginner

Advanced

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Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

Virtuoso Schematic Editor (L, XL, 2, online)

Virtuoso Visualization and Analysis XL (0.5, online)

IC 6.1.7 Virtuoso® ADE Explorer Series

- **S1** Set Up and Run Analog Simulations (0.5, online)
- **S2** Analyzing Simulations Using the ViVA XL Waveform Tool (0.5, online)
- **S3** Corner Analysis & Monte Carlo Simulations (0.5)
- **S4** Real-Time Tuning, Checks /Asserts, Reliability Analysis (0.5)

IC 6.1.7 Virtuoso® ADE Assembler Series

- **S1** Introducing the Assembler Environment (0.5, online)
- **S2** Sweeping Variables, Simulating Corners & Creating Run Plans (0.5, online)
- **S3** Circuit Checks, Device Asserts and Reliability Analysis (0.5)

Mixed-Signal Simulations using Spectre AMS Designer NEW (2, online)

Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model NEW (1)

Mixed-Signal IP & Testbench Reuse (0.5)

IC 6.1.8 Virtuoso® ADE Explorer & Assembler Series NEW

- **S1** ADE Explorer & Single Test Corner Analysis (0.5, online)
- **S2** ADE Assembler & Multi Test Corner Analysis (1, online)
- **S3** Sweeping Variables and Simulating Corners (0.5, online)
- **S4** Monte Carlo, Real-Time Tuning & Run Plans (0.5, online)

Design Checks and Asserts NEW (1, online)

Virtuoso® ADE Verifier Series NEW

- **S1** Setup, Run, View Verif. Results (1, online)
- **S2** Reference Flow and Analog Coverage Using the Setup Library Assistant (1, online)

Variation Analysis using the Variation Option (1)

Analog Modeling with Verilog-A (3, online)

- Behavioral Modeling w/ Verilog AMS (2, online)
- Behavioral Modeling with VHDL-AMS (3)
- Real Modeling with SystemVerilog (3, online)
- Real Modeling with Verilog-AMS (2, online)
- Transistor Power Signoff w/ Voltus™-Fi (1.5)

Spectre Simulator Fundamentals Series

- **S1** Spectre Basics (1, online)
- **S2** Large-Signal (0.5, online)
- **S3** Small-Signal (0.5, online)
- **S4** Spectre MDL (0.5, online)

Spectre Accelerated Parallel Simulator (APS) NEW (1, online)

Spectre XPS for Mixed-Signal Designs NEW (1, online)

Virtuoso EAD with LDE (1)

Virtuoso Spectre Pro Series

- **S1** DC Algorithm (0.5)
- **S2** AC, XF, STB, Noise (0.5)
- **S3** Transient Algorithm (0.5)
- **S4** Fourier Transform (0.5)
- **S5** Transient Noise (1)

Spectre® RF Shooting Newton (2)

Spectre® RF Harmonic Balance (2)

Virtuoso Analog Design Environment (L, 3, online)

Virtuoso® Analog Simulation Series

- T1 (XL, 1)
- T2 (XL, 0.5)
- T3 (XL, 0.5)
- T4 (GXL, 0.5)

Library Characterization

Liberate™ Characterization Portfolio (2)

- Liberate™ MX Memory Characterization (2.5)
- Liberate™ Variety™ Statistical Library Characterization (1)

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Custom IC, Analog and RF Design Learning Map

2 of 2 – see prior page

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2
- SKILL Language Programming Fundamentals — 3
- SKILL Language Programming — 5
- SKILL Development of Parameterized Cells — 2
- SKILL Programming for IC Layout Design — 2
- Advanced SKILL Language Programming — 3

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics — L, 1
- Virtuoso Connectivity-Driven Layout Transition — L, XL, 2
- Virtuoso Abstract Generator NEW — GXL, 1
- Virtuoso Floorplanner — GXL, 1
- Virtuoso Space-Based Router — GXL, 2
- Virtuoso Space-Based Router Express — GXL, 0.5

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — L, 0.5
- T2: Create and Edit Commands — L, 0.5
- T3: Basic Commands — XL, 0.5
- T4: Advanced Commands — XL, 0.5
- T5: Interactive Routing — XL, 0.5
- T6: Constraint-Driven Flow and Power Routing — XL, GXL, 0.5
- T7: Module Generator and Floorplanner — XL, GXL, 0.5
- T8: Debugging Layout Issues — L, XL, 0.5

Virtuoso® Advanced-Node Series – ICADV

- Virtuoso Layout for Advanced Nodes — 2
- T1: Place and Route NEW — 1
- T2: Electromigration NEW — 0.5

Layout Verification

- Physical Verification System (PVS) — 2
- Physical Verification Language Rules-Writer — 2

Quantus™ Extraction Solution Transistor-Level Series NEW

- T1: Overview and Technology Setup — 0.5
- T2: Parasitic Extraction — 1
- T3: Extracted View Flows and Advanced Features — 0.5

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Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis and Test

- Design For Test Fundamentals
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Synthesis Solution
- Test Synthesis Using Genus Synthesis Solution
- Advanced Synthesis with Genus Stylus Common UI
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

Implementation

- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking

- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO
- Conformal Constraint Designer

Cadence® RTL-to-GDSII Flow

Virtuoso® Digital Implementation

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Acceleration, Coverage and Debug

- Incisive® SystemC®, VHDL, and Verilog Simulation — 2
- Incisive Comprehensive Coverage with IMC — 2
- Incisive Simulation Performance Optimization NEW
- Perspec™ System Verifier - Basic — 2
- Low-Power Simulation with CPF — 2
- Low-Power Simulation with IEEE1801 UPF — 2
- Incisive Functional Safety Simulator NEW — 1
- Xcelium™ Simulator NEW — 2
- Cadence® RTL-To-GDSII Flow NEW — 2
- Foundations of Metric-Driven Verification — 1
- Xcelium Integrated Coverage NEW — 2
- Indago™ Debug Analyzer App NEW
- Metric-Driven Verification Using vManager™ NEW — 3
- vManager Tool Usage in Batch Mode — 0.5
- Specman® NEW Fundamentals for Block-level Environment Developers — 5
- Specman Advanced Verification — 4
- VIP Basic Building Blocks and Usage NEW — 2

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application (4)
  - Master VHDL For Verilog Engineers (3)
  - SystemVerilog for Design and Verification (5)
    - SystemVerilog Advanced / Accelerated Verification Using UVM (5)
      - SystemVerilog Advanced Register Verification Using UVM NEW (2)
  - Real Modeling with Verilog AMS (2)
    - Real Modeling with SystemVerilog AMS NEW (2)
- VHDL Language and Application (5)
  - Verilog for VHDL Users (2)
  - SystemVerilog Assertions (2)
    - JasperGold® Formal Fundamentals NEW (3)
  - Verification with PSL (2)
- C++ Language Fundamentals for Design and Verification (2)
  - SystemC® Language Fundamentals (3)
    - SystemC Synthesis with Stratus HLS NEW (3)
    - SystemC Transaction-Level Modeling TLM2.0 (2)
    - Perl for EDA Engineering (3)
    - Tcl Scripting for EDA + Intro to Tk (3)

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Tensilica Processor IP Learning Map

Tensilica Processors

- Tensilica® Processor Fundamentals — 2 day(s), Online Course Available
- Tensilica Xtensa® Processor Interfaces — Online Course Available
- Tensilica Xtensa Hardware Verification and EDA — Online Course Available
- Tensilica Instruction Extension Language and Design — 1 day(s), Online Course Available
- Introduction to System Modeling with Tensilica Processor Cores — 1 day(s), Online Course Available

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine — 2 day(s)
- Tensilica ConnX BBE32EP Baseband Engine — 2 day(s), Online Course Available
- Tensilica ConnX BBE64EP Baseband Engine — 2 day(s)

Fusion DSP

- Tensilica Fusion F1 DSP — Online Course Available
- Tensilica Fusion G3 DSP — 2 day(s), Online Course Available
- Tensilica Fusion G6 DSP — 2 day(s)

HiFi Audio DSP

- Tensilica Audio Codec API — 0.5 day(s)
- Tensilica HiFi 2/EP/Mini Audio Engine ISA — Online Course Available
- Tensilica HiFi 3 Audio Engine ISA — 1 day(s), Online Course Available
- Tensilica HiFi 4 DSP — NEW — 1 day(s)

Vision DSP

- Tensilica Vision P5 DSP — 2 day(s), Online Course Available
- Tensilica Vision P6 DSP — 2 day(s), Online Course Available
- Tensilica Vision C5 DSP — NEW — 1 day(s), Online Course Available

NEW New Course | # Number of days for instructor-led course | Online Course Available