Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
  - Beginner
  - Number of days for instructor-led course: 3
  - Tiers of Cadence products used in course: L

- **Allegro Design Entry HDL Basics**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro System Design Authoring**
  - Beginners
  - Two new courses added
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro Design Reuse**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Allegro AMS Simulator**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

## PCB Design
- **Allegro Design Entry Using OrCAD® Capture**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **OrCAD CIS**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Allegro Team Design Authoring**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Allegro Design Workbench for Engineers and Designers**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Analog Simulation with PSpice®**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Allegro PCB Editor Basic Techniques**
  - Beginners
  - Number of days for instructor-led course: 3
  - Tiers of Cadence products used in course: L

- **Allegro PCB Router Basics**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro PCB Editor Intermediate Techniques**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro PCB Editor Advanced Methodologies**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Allegro Update Training**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

## SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
  - Beginners
  - Number of days for instructor-led course: 3
  - Tiers of Cadence products used in course: L

- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro Sigiry™ SI Foundations**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro Sigiry PI**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Sigiry PowerDC™ and OptimizePI™**
  - Beginners
  - Number of days for instructor-led course: 1
  - Tiers of Cadence products used in course: L

- **Sigiry SystemSI™ for Parallel Bus and Serial Link Analysis**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Sigiry PowerSI® for Model Generation and Analysis**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

## Library Development
- **Allegro PCB Librarian**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro Design Workbench for Librarians**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro Design Workbench for Administrators**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

- **Allegro PCB Editor SKILL Programming Language**
  - Beginners
  - Number of days for instructor-led course: 3
  - Tiers of Cadence products used in course: L

- **Allegro Tool Setup and Configuration**
  - Beginners
  - Number of days for instructor-led course: 2
  - Tiers of Cadence products used in course: L

© 2017 Cadence Design Systems, Inc.
<table>
<thead>
<tr>
<th>IC Package Design</th>
<th>SI/PI Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td>Allegro Sigrity™ SI Foundations</td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td>Allegro Sigrity PI</td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td>Sigtry PowerDC™ and OptimizePI™</td>
</tr>
<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
<td>Sigtry SystemSI™ for Parallel Bus and Serial Link Analysis</td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td>Sigtry PowerSI® for Model Generation and Analysis</td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td><strong>NEW</strong></td>
</tr>
</tbody>
</table>
Digital Design and Signoff Learning Map

**Synthesis**
- Genus™ Synthesis Solution
- Low-Power Synthesis Flow with Genus Synthesis Solution
- Test Synthesis Using Genus Synthesis Solution
- Advanced Synthesis with Genus Synthesis Solution
- Fundamentals of IEEE 1801 Low-Power Specification Flow
- Modus DFT Software Solution
- Joules™ Power Calculator

**Implementation**
- Virtuoso® Digital Implementation
- Innovus™ Implementation System
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Logic Equivalence Checking with Conformal® EC
- Conformal Low-Power Verification
- Conformal ECO
- Conformal Constraint Designer

**Cadence® RTL-to-GDS Flow**

© 2017 Cadence Design Systems, Inc.
System Design and Verification Learning Map

Design and Verification Languages

- **Verilog Language and Application**
  - Master VHDL For Verilog Engineers
  - SystemVerilog Advanced / Accelerated Verification Using UVM
  - SystemVerilog Advanced Register Verification Using UVM

- **VHDL Language and Application**
  - Verilog for VHDL Users
  - SystemVerilog Assertions
  - JasperGold® Formal Fundamentals

- **C++ Language Fundamentals for Design and Verification**

- **SystemC® Language Fundamentals**
  - SystemC Synthesis with Stratus HLS
  - SystemC Transaction-Level Modeling TLM2.0

- **Real Modeling with Verilog AMS**
  - Real Modeling with SystemVerilog AMS

- **SystemVerilog for Design and Verification**

- **Verification with PSL**

- **Perl for EDA Engineering**

- **Tcl Scripting for EDA + Intro to Tk**

**New Course**

- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available

© 2017 Cadence Design Systems, Inc.
# Tensilica Processor IP Learning Map

<table>
<thead>
<tr>
<th>Tensilica Processors</th>
<th>ConnX DSP</th>
<th>Fusion DSP</th>
<th>HiFi Audio DSP</th>
<th>Vision DSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tensilica® Processor Fundamentals</td>
<td>Tensilica ConnX BBE16EP Baseband Engine</td>
<td>Tensilica Fusion F1 DSP</td>
<td>Tensilica Audio Codec API</td>
<td>Tensilica Vision P5 DSP</td>
</tr>
<tr>
<td>Tensilica Xtensa® Processor Interfaces</td>
<td>Tensilica ConnX BBE32EP Baseband Engine</td>
<td>Tensilica Fusion G3 DSP</td>
<td>Tensilica HiFi 2/EP/Mini Audio Engine ISA</td>
<td>Tensilica Vision P6 DSP</td>
</tr>
<tr>
<td>Tensilica Xtensa Hardware Verification and EDA</td>
<td>Tensilica ConnX BBE64EP Baseband Engine</td>
<td>Tensilica Fusion G6 DSP</td>
<td>Tensilica HiFi 3 Audio Engine ISA</td>
<td>Tensilica Vision C5 DSP</td>
</tr>
<tr>
<td>Tensilica Instruction Extension Language and Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Introduction to System Modeling with Tensilica Processor Cores</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

© 2017 Cadence Design Systems, Inc.