Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
- **Allegro Design Entry HDL Basics**
- **Allegro System Capture**
- **Allegro System Architect**
- **Allegro Design Reuse**
- **Allegro AMS Simulator**
- **Allegro AMS Simulator Advanced Analysis**

## PCB Design
- **Allegro PCB Editor Basic Techniques**
- **OrCAD® Capture**
- **OrCAD Capture Constraint Manager PCB Flow**
- **Allegro EDM Design Entry HDL Front-to-Back Flow**
- **Allegro Team Design Authoring**
- **Analog Simulation with PSpice®**
- **Allegro PCB Editor Intermediate Techniques**
- **Allegro PCB Router Basics**
- **Allegro PCB Editor Advanced Methodologies**
- **Allegro High-Speed Constraint Management**
- **Allegro Update Training**
- **Analog Simulation with PSpice Advanced Analysis**
- **Advanced Design Verification with the RAVEL Programming Language**

## SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
- **Allegro Sigtry™ SI Foundations**
- **Allegro Sigtry PI**
- **Sigrity PowerDC™ and OptimizePI™**
- **Sigrity Aurora**
- **TopXplorer SystemSI for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**
- **Clarity 3D Solver**
- **Celsius Thermal Solver**

## Library Development
- **Allegro PCB Librarian**
- **Allegro EDM PCB Librarian**
- **Allegro Design Entry HDL SKILL® Programming Language**
- **Allegro PCB Editor SKILL Programming Language**

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**New Course** | **Number of days for instructor-led course** | **Tiers of Cadence products used in course** | **Online Course Available** | **Digital Badge Available**
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System Design and Verification Learning Map

Design and Verification Languages

- **Verilog Language and Application**
  - Real Modeling with Verilog AMS
  - Real Modeling with SystemVerilog
  - SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
- **SystemVerilog for Design and Verification**
  - UVM
    - Essential SystemVerilog for UVM (optional)
    - SystemVerilog Accelerated Verification Using UVM
- **SystemVerilog for Design and Verification**
  - SystemVerilog for Design and Verification
  - SystemVerilog Assertions
  - JasperGold® Formal Fundamentals
  - SVA, Formal & JasperGold® Fundamentals for Designers
- **VHDL Language and Application**
  - VHDL Language and Application
- **C++ Language Fundamentals for Design and Verification**
  - C++ Language Fundamentals

- **SystemC® Language Fundamentals**
  - SystemC Synthesis with Stratus HLS
  - SystemC Transaction-Level Modeling TLM2.0

- **SystemVerilog Advanced Register Verification Using UVM**
- **JasperGold® Formal Expert**

NEW Course
Number of days for instructor-led course
Tiers of Cadence products used in course
Online Course Available
Digital Badge Available
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Real Modeling with Verilog AMS
Real Modeling with SystemVerilog
SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
Perl for EDA Engineering
Tcl Scripting for EDA

Essential SystemVerilog for UVM (optional)
SystemVerilog Accelerated Verification Using UVM
SystemVerilog Advanced Register Verification Using UVM
SystemVerilog for Design and Verification
SystemVerilog Assertions
JasperGold® Formal Fundamentals
SVA, Formal & JasperGold® Fundamentals for Designers