

Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

PCB Design and Analysis Learning Map

Beginner

Advanced

Beginner

Advanced



IC Package Design and Analysis Learning Map

Beginner



Advanced

IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis **NEW**



Sigrity PowerSI® for Model Generation and Analysis



Beginner



Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

Beginner

Advanced

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

Virtuoso® Analog Design Environment



Virtuoso Analog Simulation Series

- T1** The Virtuoso Analog Design XL Environment
- T2** Creating Sweeps and Running Corner Analysis
- T3** Monte Carlo Simulation Using ADE XL
- T4** Sensitivity Analysis and Circuit Optimization Using ADE GXL

- Mixed-Signal Simulations using Spectre AMS Designer
- Mixed-Signal IP & Testbench Reuse
- Analog Modeling with Verilog-A
- Behavioral Modeling with / Verilog-AMS / VHDL-AMS
- Real Modeling with / SystemVerilog / Verilog-AMS
- Transistor-Level Power Signoff with Voltus™-Fi

Virtuoso Schematic Editor



Virtuoso® ADE Explorer Series

- S1** Set Up and Run Analog Simulations Using the Spectre® Simulator
- S2** Analyzing Simulations Using the ViVA XL Waveform Tool
- S3** Corner Analysis and Monte Carlo Simulations
- S4** Real-Time Tuning, Checks/Asserts, and Reliability Analysis

Virtuoso ADE Assembler Series

- S1** Introducing the Assembler Environment
- S2** Sweeping Variables, Simulating Corners and Creating Run Plans
- S3** Circuit Checks, Device Asserts and Reliability Analysis

- Virtuoso ADE Verifier
- Variation Analysis Using the Virtuoso Variation Option

Spectre Simulator Fundamentals Series

- S1** Spectre Basics
- S2** Large-Signal
- S3** Small-Signal
- S4** Spectre MDL

- Design Checks & Asserts
- Spectre Accelerated Parallel Simulator (APS)
- Spectre XPS for Mixed-Signal Designs
- Virtuoso EAD with LDE

Virtuoso Spectre Pro Series

- S1** DC Algorithm
- S2** AC, XF, STB, Noise
- S3** Transient Algorithm
- S4** Fourier Transform
- S5** Transient Noise

- Spectre® RF/ Shooting Newton / Harmonic Balance

Library Characterization

- Cadence® Library Characterization and Validation
- Virtuoso Liberate™ MX for Memory Characterization
- Cadence Variety™ Statistical Library Characterization

Beginner

Advanced

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction
- SKILL Language Programming Fundamentals
- SKILL Language Programming
- SKILL Development of Parameterized Cells
- SKILL Programming for IC Layout Design
- Advanced SKILL Language Programming

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics
- Virtuoso Connectivity-Driven Layout Transition
- Virtuoso Abstract Generator
- Virtuoso Floorplanner
- Virtuoso Space-Based Router
- Virtuoso Space-Based Router Express
- Virtuoso® Advanced-Node Series – ICADV
 - Virtuoso Layout for Advanced Nodes
 - T1: Place and Route
 - T2: Electromigration

Layout Verification

- Physical Verification System (PVS)
- Physical Verification Language Rules-Writer
- Quantus™ QRC Transistor-Level Series
 - T1: Overview and Technology Setup
 - T2: Parasitic Extraction
 - T3: Extracted View Flows and Advanced Features

Digital Design and Signoff Learning Map

Beginner

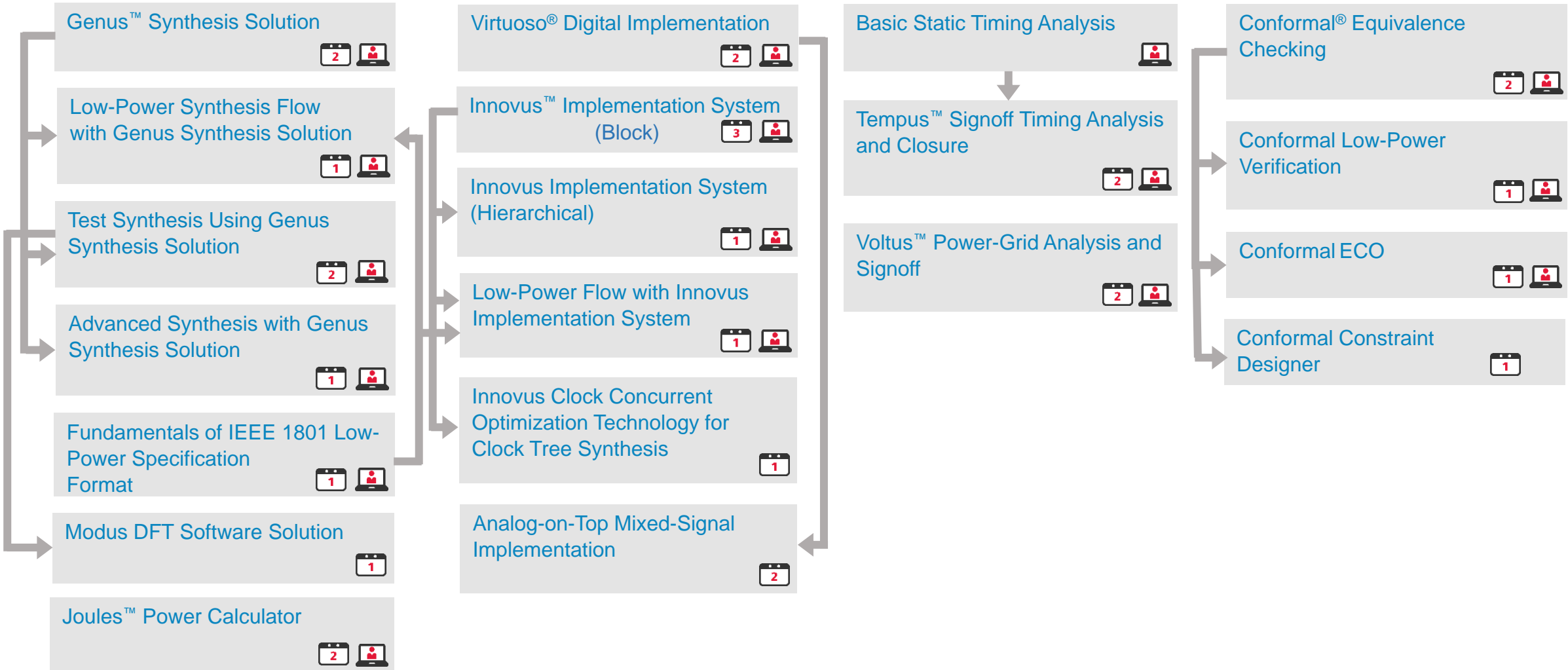
Advanced

Beginner

Advanced

Synthesis Implementation Silicon Signoff Equivalence Checking

Cadence® RTL-to-GDS Flow 2



System Design and Verification Learning Map

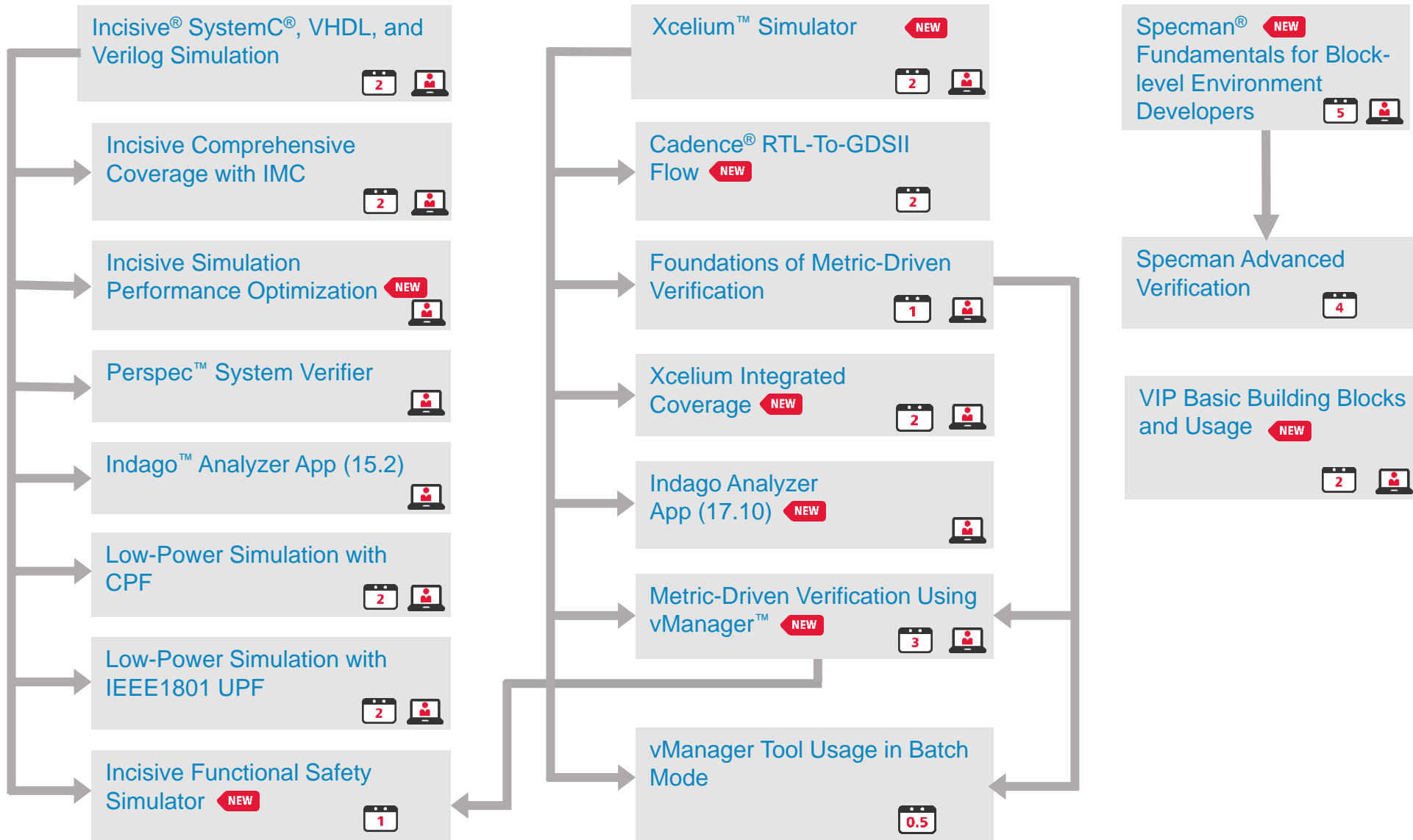
Beginner

Advanced

Beginner

Advanced

Simulation, Acceleration, Coverage and Debug



System Design and Verification Learning Map

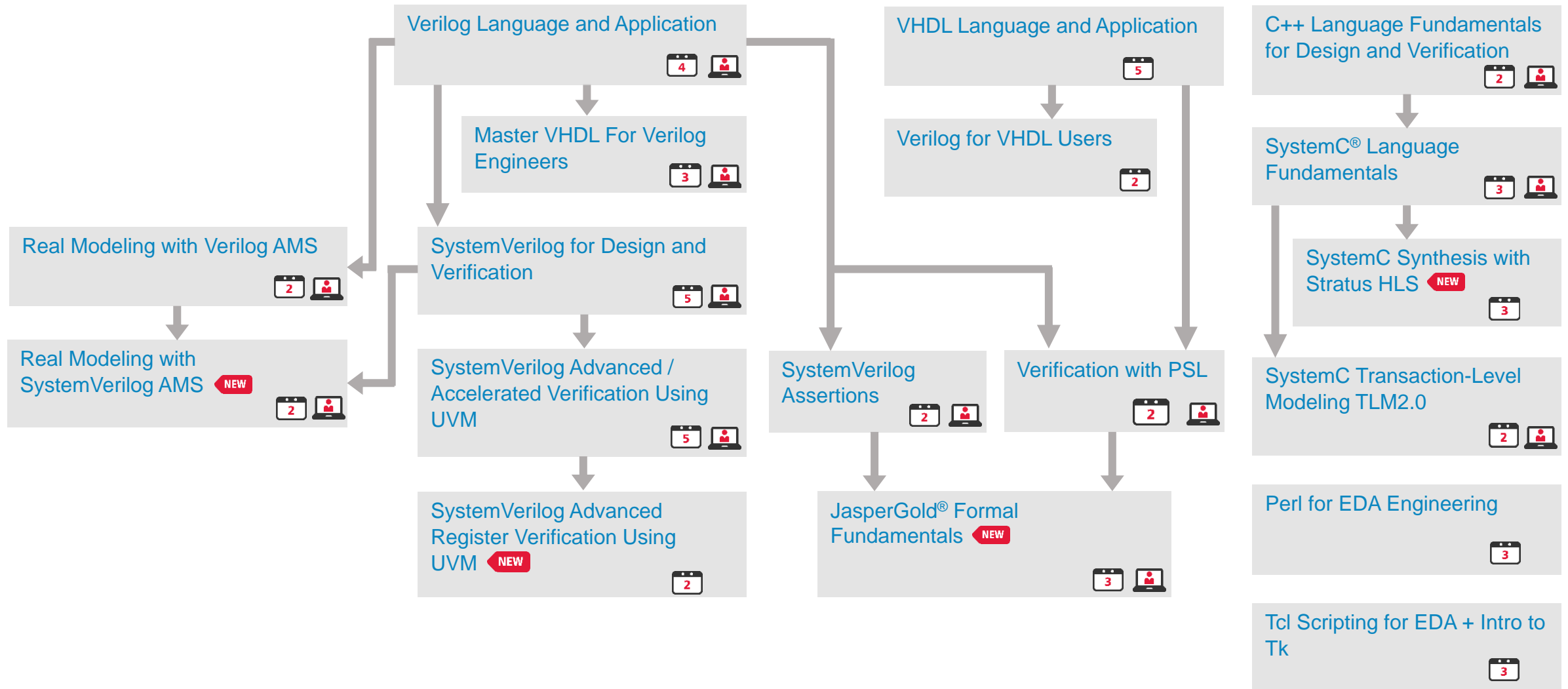
Beginner

Advanced

Beginner

Advanced

Design and Verification Languages



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

Tensilica Processor IP Learning Map

Tensilica Processors

ConnX DSP

Fusion DSP

HiFi Audio DSP

Vision DSP

Tensilica® Processor Fundamentals



Tensilica Xtensa® Processor Interfaces



Tensilica Xtensa Hardware Verification and EDA



Tensilica Instruction Extension Language and Design



Introduction to System Modeling with Tensilica Processor Cores



Tensilica ConnX BBE16EP Baseband Engine



Tensilica ConnX BBE32EP Baseband Engine



Tensilica ConnX BBE64EP Baseband Engine



Tensilica Fusion F1 DSP



Tensilica Fusion G3 DSP



Tensilica Fusion G6 DSP



Tensilica Audio Codec API



Tensilica HiFi 2/EP/Mini Audio Engine ISA



Tensilica HiFi 3 Audio Engine ISA



Tensilica HiFi 4 DSP **NEW**



Tensilica Vision P5 DSP



Tensilica Vision P6 DSP



Tensilica Vision C5 DSP **NEW**



New Course



Number of days for instructor-led course



Online Course Available

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