Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
## PCB Design and Analysis Learning Map

**Logic Design**
- Allegro Design Entry HDL Front-to-Back Flow
- Allegro System Architect
- Allegro Design Reuse
- Allegro AMS Simulator
- Allegro Design Entry HDL Basics
- Allegro System Capture

**PCB Design**
- Allegro PCB Editor Basic Techniques
- Allegro PCB Editor Advanced Methodologies
- Allegro PCB Editor Intermediate Techniques
- Allegro PCB Router Basics
- Allegro Update Training
- Advanced Design Verification with the RAVEL Programming Language
- Analog Simulation with PSpice Advanced Analysis

**SI/PI Analysis**
- Essential High-Speed PCB Design for Signal Integrity
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
- Allegro Sigrity™ SI Foundations
- Allegro Sigrity PI
- Sigtry PowerDC™ and OptimizePI™
- Sigtry Aurora
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM
- Clarity 3D Solver
- Celsius Thermal Solver

**Library Development**
- Allegro PCB Librarian
- Allegro EDM PCB Librarian
- Allegro Design Entry HDL SKILL® Programming Language
- Allegro PCB Editor SKILL Programming Language

### Course Information
- **New Course**
- **Number of days for instructor-led course**
- **Tiers of Cadence products used in course**
- **Online Course Available**
- **Digital Badge Available**

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# IC Package Design and Analysis Learning Map

## IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
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<th>Number of days for instructor-led course</th>
<th>Tiers of Cadence products used in course</th>
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<tr>
<td>SiP Layout</td>
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<td>Allegro® Package Designer</td>
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<td>Allegro FPGA System Planner</td>
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<td>Allegro Sigrity Package Assessment and Model Extraction</td>
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<td>OrbitIO™ System Planner</td>
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<td>Advanced Design Verification with the RAVEL Programming Language</td>
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<td>Allegro Package Designer Plus</td>
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## SI/PI Analysis

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<tr>
<td>Allegro Sigrity™ SI Foundations</td>
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<td>Celsius Thermal Solver</td>
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Custom IC, Analog and RF Design Learning Map

Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

Analog Modeling with Verilog-A

Mixed-Signal Simulations using Spectre AMS Designer

Command-Line Based Mixed-Signal Simulations w/ Xcelium
Use Model

SimVision for Debugging Mixed-Signal Simulations

Behavioral Modeling with Verilog AMS

Behavioral Modeling with VHDL-AMS

Real Modeling with Verilog-AMS

Real Modeling with SystemVerilog

SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

Virtuoso Schematic Editor

Virtuoso Visualization and Analysis

Virtuoso® ADE Explorer & Assembler Series

S1 ADE Explorer & Single Test Corner Analysis

S2 ADE Assembler & Multi Test Corner Analysis

S3 Sweeping Variables and Simulating Corners

S4 Monte Carlo, Real-Time Tuning & Run Plans

Virtuoso® ADE Verifier Series

S1 Setup, Run, & View Verifier Results

S2 Reference Flow and Analog Coverage Using the Setup Library Assistant

Virtuoso® Spectre® Pro Series

S1 DC Algorithm

S2 AC, XF, STB, Noise

S3 Transient Algorithm

S4 Fourier Transform

S5 Transient Noise

Spectre® RF Shooting Newton

Spectre® RF Harmonic Balance

5G mmWave Handset System Design – S1 RFIC (Transceiver) Design

Spectre® Simulator Fundamentals Series

S1 Spectre Basics

S2 Large-Signal Analysis

S3 Small-Signal Analysis

S4 Spectre MDL

Design Checks and Asserts

High Performance Spectre Simulation

Fundamentals Series

S1 Spectre Basics

S2 Large-Signal Analysis

S3 Small-Signal Analysis

S4 Spectre MDL

Advanced

Beginner

New Course

Number of days for instructor-led course

Tiers of Cadence products used in course

Online Course Available

Digital Badge Available

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Digital Design and Signoff Learning Map

**Synthesis and Test**
- Design For Test Fundamentals
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Stylus Common UI
- Test Synthesis with Genus Stylus Common UI
- Advanced Synthesis with Genus Stylus Common UI
- Modus DFT Software Solution
- Joules™ Power Calculator

**Implementation**
- Innovus Block Implementation with Stylus Common UI
- Innovus Hierarchical Implementation with Stylus Common UI
- Innovus Low-Power Flow with Stylus Common UI
- Innovus Clock Concurrent Optimization Technology with Stylus Common UI

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure with Stylus Common UI
- Voltus™ Power Grid Analysis and Signoff with Stylus Common UI

**Equivalence Checking**
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal Low-Power Verification Using IEEE1801
- Conformal ECO

**Cadence® RTL-to-GDSII Flow**

- New Course
- Number of days for instructor-led course
- Online Course Available
- Digital Badge Available

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System Design and Verification Learning Map

Design and Verification Languages

Verilog Language and Application
- Real Modeling with Verilog AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
- Perl for EDA Engineering
- Tcl Scripting for EDA

SystemVerilog for Design and Verification
- UVM
- Essential SystemVerilog for UVM (optional)
- SystemVerilog Accelerated Verification Using UVM
- SystemVerilog Advanced Register Verification Using UVM

SystemVerilog Assertions
- JasperGold® Formal Fundamentals
- JaspeGold® Formal Expert

VHDL Language and Application

C++ Language Fundamentals for Design and Verification
- SystemC® Language Fundamentals
- SystemC Synthesis with Stratus HLS
- SystemC Transaction-Level Modeling TLM2.0

SystemVerilog for Design and Verification
- Essential SystemVerilog for UVM (optional)
- SystemVerilog Accelerated Verification Using UVM
- SystemVerilog Advanced Register Verification Using UVM

C++ Language Fundamentals for Design and Verification
- SystemC® Language Fundamentals
- SystemC Synthesis with Stratus HLS
- SystemC Transaction-Level Modeling TLM2.0

Digital Badge Available

Real Modeling with Verilog AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
- Perl for EDA Engineering
- Tcl Scripting for EDA

Digital Badge Available

JasperGold® Formal Expert
- SVA, Formal & JasperGold® Fundamentals for Designers

New Course
- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available
- Digital Badge Available

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Tensilica Processor IP Learning Map

Tensilica Xtensa LX
- Processor Fundamentals
- Processor Interfaces
- Hardware Verification and EDA
- Instruction Language and Design
- System Modeling using XTSC

ConnX DSP
- BBE16EP Baseband Engine
- BBE32EP Baseband Engine
- BBE64EP Baseband Engine
- ConnX 110 and 120 DSP Family

Fusion & FloatingPoint DSP
- Fusion F1 DSP
- Fusion G3 DSP
- Fusion G6 DSP
- FloatingPoint DSP Family

HiFi Audio DSP
- Audio Codec API
- HiFi 2/EP/Mini Audio Engine ISA
- HiFi 3 Audio Engine ISA
- HiFi 4 DSP

Vision DSP
- Vision DSP Family
- Xpansion Network Compiler v2
- DNA 100 Architecture and Programming

New Course
Number of days for instructor-led course
Online Course Available
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Tensilica Processor IP Learning Map

Tensilica Xtensa NX
- Tensilica® Xtensa® NX Processor Fundamentals
- Tensilica Xtensa NX Processor Interfaces
- Tensilica Instruction Extension Language and Design
- Tensilica System Modeling using XTSC

ConnX DSP
- Tensilica ConnX B10 DSP
- Tensilica ConnX B20 DSP

Vision DSP
- Tensilica Vision DSP Family
- Tensilica Xtensa Neural Network Compiler v2

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