Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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### IC Package Design

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### SI/PI Analysis

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Custom IC, Analog and RF Design Learning Map

Circuit Design, Simulation, Modeling and RF Design

Virtuoso Schematic Editor
IC 6.1.7 Virtuoso® ADE Explorer Series
S1 Set Up and Run Analog Simulations
S2 Analyzing Simulations Using the ViVA XL WaveformViewer
S3 Corner Analysis & Monte Carlo Simulations
S4 Real-Time Tuning, Checks /Asserts, Reliability Analysis

Virtuoso Visualization and Analysis XL
IC 6.1.8 Virtuoso® ADE Explorer & Assembler Series
S1 ADE Explorer & Single Test Corner Analysis
S2 ADE Assembler & Multi Test Corner Analysis
S3 Sweeping Variables and Simulating Corners
S4 Monte Carlo, Real-Time Tuning & Run Plans

Design Checks and Asserts
Virtuoso® ADE Verifier Series
S1 Setup, Run, View Verif. Results
S2 Reference Flow and Analog Coverage Using the Setup Library Assistant
Variation Analysis using the Variation Option

Analog Modeling with Verilog-A
Behavioral Modeling with Verilog-AMS
Behavioral Modeling with VHDL-AMS
Real Modeling with SystemVerilog
Real Modeling with Verilog-AMS
Transistor Power Signoff w/ Voltus™-Fi

Spectre Simulator Fundamentals Series
S1 Spectre Basics
S2 Large-Signal
S3 Small-Signal
S4 Spectre MDL

Spectre Accelerated Parallel Simulator (APS)
Spectre XPS for Mixed-Signal Designs
Virtuoso EAD with LDE

Virtuoso Spectre Pro Series
S1 DC Algorithm
S2 AC, XF, STB, Noise
S3 Transient Algorithm
S4 Fourier Transform
S5 Transient Noise

Spectre® RF Shooting Newton
Spectre® RF Harmonic Balance

Virtuoso Analog Design Environment
Virtuoso® Analog Simulation Series
T1 XL
T2 XL
T3 XL
T4 XL

Library Characterization
Liberate™ Characterization Portfolio
Liberate™ MX Memory Characterization
Liberate™ Variety™ Statistical Library Characterization

New Course
1 of 2 – see next page
Number of days for instructor-led course
Tiers of Cadence products used in course
Online Course Available
Digital Badge Available
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System Design and Verification Learning Map

Simulation, Acceleration, Coverage and Debug

Incisive® SystemC®, VHDL, and Verilog Simulation
- Incisive Comprehensive Coverage with IMC
- Incisive Simulation Performance Optimization
- Perspec™ System Verifier - Basic
- Low-Power Simulation with CPF
- Low-Power Simulation with IEEE1801 UPF
- Incisive Functional Safety Simulator

Xcelium™ Simulator
- Cadence® RTL-To-GDSII Flow
- Foundations of Metric-Driven Verification
- Xcelium Integrated Coverage
- Indago™ Debug Analyzer App
- Metric-Driven Verification Using vManager™
- vManager Tool Usage in Batch Mode

Specman® Fundamentals for Block-level Environment Developers
- Specman Advanced Verification
- VIP Basic Building Blocks and Usage

Advanced
- New Course
- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available

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