

# Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

## Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

# PCB Design and Analysis Learning Map

Beginner

Advanced


















Beginner

Advanced

## Logic Design

Allegro® Design Entry HDL Front-to-Back Flow  	Allegro Design Entry Using OrCAD® Capture  
Allegro Design Entry HDL Basics  	OrCAD CIS 
Allegro System Architect  	Allegro Team Design Authoring  
Allegro Design Reuse  	Allegro Design Workbench for Engineers and Designers  
Allegro FPGA System Planner  	
Allegro AMS Simulator 	Analog Simulation with PSpice®  
Allegro AMS Simulator Advanced Analysis  	Analog Simulation with PSpice Advanced Analysis  












## PCB Design

Allegro PCB Editor Basic Techniques  
Allegro PCB Editor Intermediate Techniques  
Allegro PCB Router Basics  
Allegro PCB Editor Advanced Methodologies   
Allegro High-Speed Constraint Management  
Allegro Update Training   
Advanced Design Verification with the RAVEL Programming Language   

## SI/PI Analysis

Essential High-Speed PCB Design for Signal Integrity 
PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials 
Allegro Sigrity™ SI Foundations  
Allegro Sigrity PI  
Sigrity PowerDC™ and OptimizePI™  
Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis   
Sigrity PowerSI® for Model Generation and Analysis  

## Library Development

Allegro PCB Librarian  
Allegro Design Workbench for Librarians 
Allegro Design Workbench for Administrators  
Allegro Design Entry HDL SKILL® Programming  
Allegro PCB Editor SKILL Programming Language  
Allegro Tool Setup and Configuration  

# IC Package Design and Analysis Learning Map

Beginner



Advanced

## IC Package Design

SiP Layout



Allegro® Package Designer



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



## SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis **NEW**



Sigrity PowerSI® for Model Generation and Analysis



Beginner



Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

Beginner

Advanced

Beginner

Advanced

## Circuit Design, Simulation, Modeling and RF Design

Virtuoso® Analog Design Environment

Virtuoso Schematic Editor

**Virtuoso Analog Simulation Series**

- T1: Introduction to the Virtuoso ADE XL Environment**
- T2: Creating Sweeps and Running Corners**
- T3: Monte Carlo Simulation Using ADE XL**
- T4: Sensitivity Analysis and Circuit Optimization with ADE GXL**

**Virtuoso® ADE Explorer Series**

- S1: Set Up and Run Analog Simulations Using the Spectre® Simulator**
- S2: Analyzing Simulations Using ViVA XL**
- S3: Corner Analysis and Monte Carlo Simulation**
- S4: Real-Time Tuning, Checks/Asserts, and Reliability Analysis**

Mixed-Signal Simulations Using AMS Designer

**Virtuoso ADE Assembler Series**

- S1: Introducing the Assembler Environment**
- S2: Sweeping Variables, Simulating Corners and Creating Run Plans**
- S3: Corner Analysis and Monte Carlo Simulation**

Analog Modeling with Verilog-A

Behavioral Modeling with / Verilog-AMS / VHDL-AMS

Real Modeling with / SystemVerilog / Verilog-AMS

Transistor-Level Power Signoff with Voltus™-Fi

Virtuoso ADE Verifier

Variation Analysis Using the Virtuoso ADE Assembler

**Spectre Simulator Fundamentals Series**

- S1: Spectre Basics**
- S2: Large-Signal**
- S3: Small-Signal**
- S4: Spectre MDL**

High-Performance Simulation Using Spectre APS and XPS

Spectre APS

Virtuoso Electrically-Aware Design with LDE

**Virtuoso Spectre Pro Series**

- S1: DC Algorithm**
- S2: AC, XF, STB, Noise**
- S3: Transient Algorithm**
- S4: Fourier Transform**
- S5: Transient Noise**

Spectre® RF/Shooting Newton / Harmonic Balance

## Library Characterization

Cadence® Library Characterization and Validation

Virtuoso Liberate™ MX Memory Characterization

Cadence Variety™ Statistical Library Characterization

Beginner

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## IC CAD

- SKILL® Language Programming Introduction
- SKILL Language Programming Fundamentals
- SKILL Language Programming
- SKILL Development of Parameterized Cells
- SKILL Programming for IC Layout Design
- Advanced SKILL Language Programming

## Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics
- Virtuoso Connectivity-Driven Layout Transition
- Virtuoso Abstract Generator
- Virtuoso Floorplanner
- Virtuoso Space-Based Router
- Virtuoso Space-Based Router Express
- Virtuoso® Advanced-Node Series – ICADV
  - Virtuoso Layout for Advanced Nodes
  - T1: Place and Route
  - T2: Electromigration

## Layout Verification

- Physical Verification System (PVS)
- Physical Verification Language Rules-Writer
- Quantus™ QRC Transistor-Level Series
  - T1: Overview and Technology Setup
  - T2: Parasitic Extraction
  - T3: Extracted View Flows and Advanced Features
- Assura® Verification DRC/LVS
- Assura Rules-Writer

# Digital Design and Signoff Learning Map

Beginner

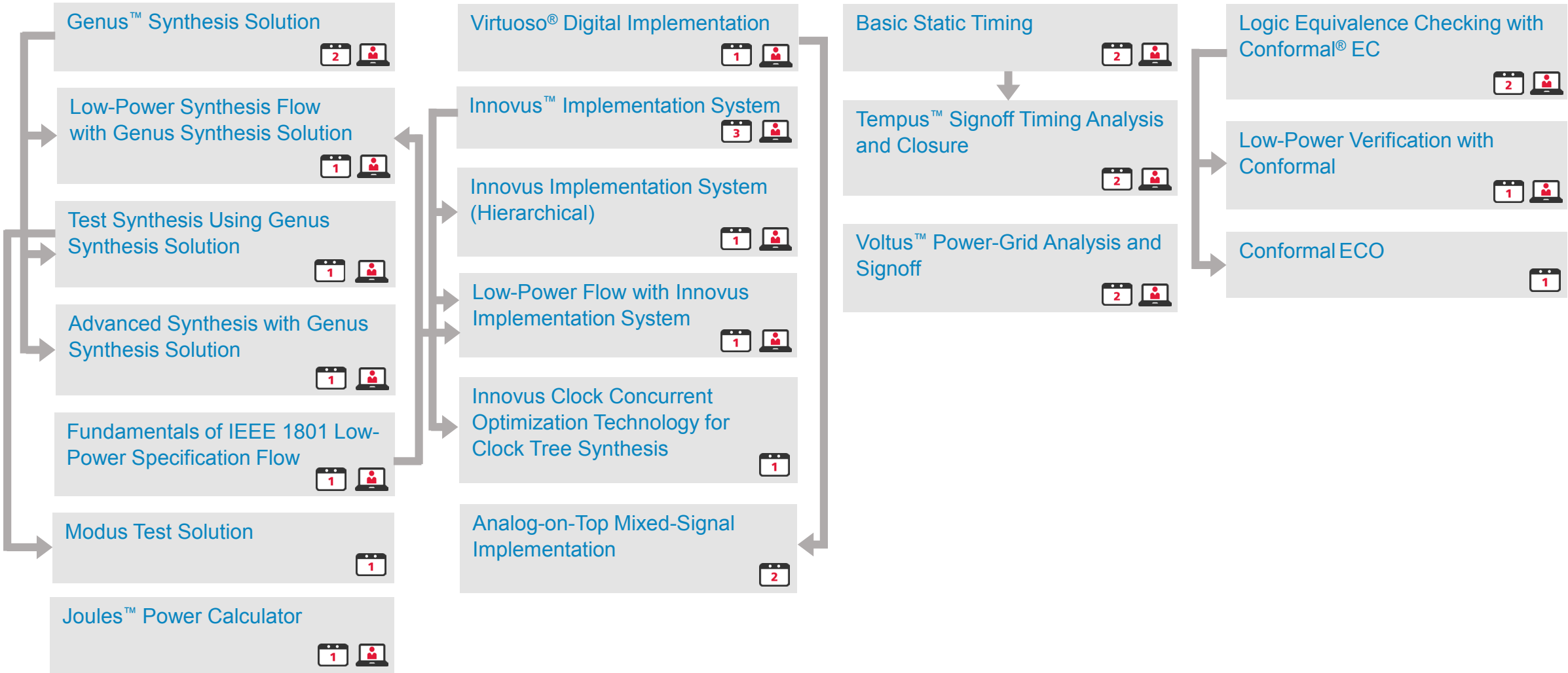
Advanced

Beginner

Advanced

## Synthesis Implementation Silicon Signoff Equivalence Checking

Cadence® RTL-to-GDS Flow 2



# System Design and Verification Learning Map

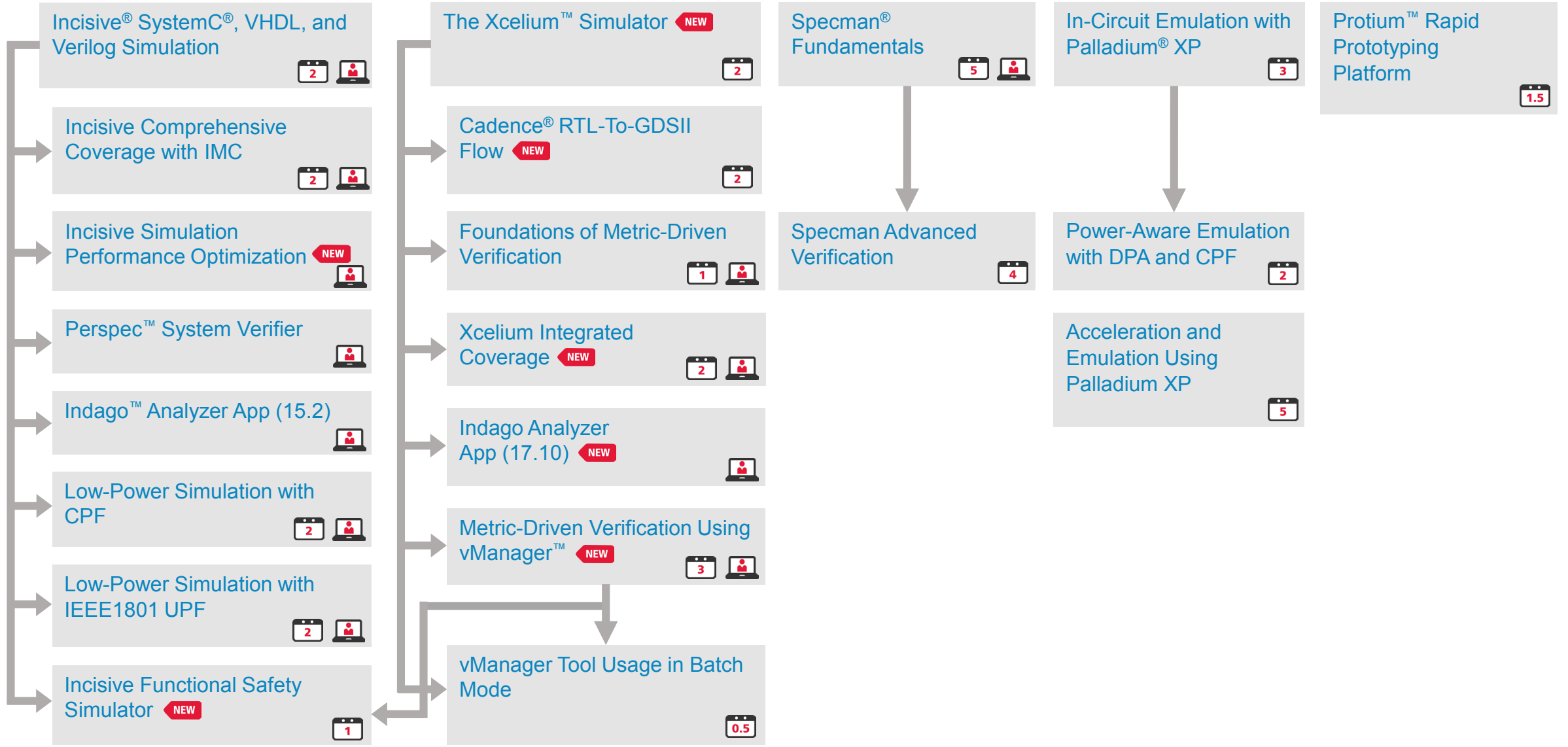
Beginner

Advanced

Beginner

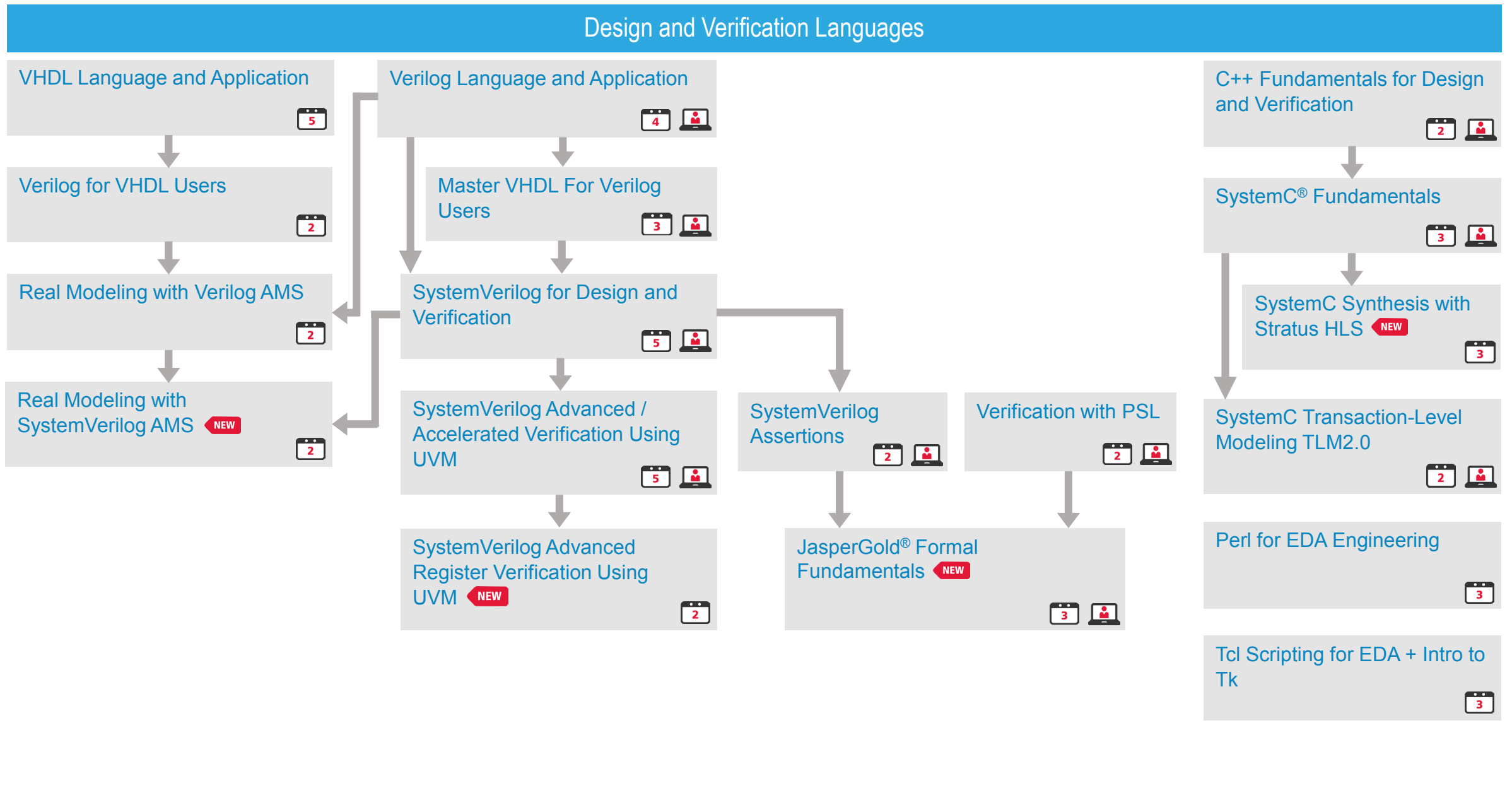
Advanced

## Simulation, Acceleration, Emulation, Coverage and Debug



# System Design and Verification Learning Map

Beginner



Beginner

Advanced

Advanced



# Tensilica Processor IP Learning Map

## Tensilica Processors

Tensilica® Processor Fundamentals



## ConnX DSP

Tensilica ConnX BBE16EP Baseband Engine



Tensilica ConnX BBE32EP Baseband Engine



Tensilica ConnX BBE64EP Baseband Engine



## Fusion DSP

Tensilica Fusion F1 DSP



Tensilica Fusion G3 DSP



Tensilica Fusion G6 DSP



## HiFi Audio DSP

Tensilica Audio Codec API



Tensilica HiFi 2/EP/Mini Audio Engine ISA



Tensilica HiFi 3 Audio Engine ISA



Tensilica HiFi 4 DSP **NEW**



## Vision DSP

Tensilica Vision P5 DSP



Tensilica Vision P6 DSP



Tensilica Vision C5 DSP **NEW**



Tensilica Xtensa® Processor Interfaces



Tensilica Xtensa Hardware Verification and EDA



Tensilica Instruction Extension Language and Design



Introduction to System Modeling with Tensilica Processor Cores



**cā dence<sup>®</sup>**