Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
### IC Package Design

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<th>Cadence Products</th>
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<td>Allegro® Package Designer</td>
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<td>OrbitIO™ System Planner</td>
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<td>Advanced Design Verification with the RAVEL Programming Language</td>
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### SI/PI Analysis

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<td>Celsius Thermal Solver</td>
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### Digital Design and Signoff Learning Map

**Synthesis and Test**
- **Advanced Synthesis with Genus Stylus Common UI**
- **Fundamentals of IEEE 1801 Low-Power Specification Format**
- **Modus DFT Software Solution**
- **Joules™ Power Calculator**

**Implementation**
- **Genus™ Synthesis Solution with Stylus Common UI**
- **Low-Power Synthesis Flow with Genus Stylus Common UI**
- **Test Synthesis with Genus Stylus Common UI**
- **Virtuoso® Digital Implementation**

**Silicon Signoff**
- **Innovus Implementation System (Block)**
- **Innovus Implementation System (Hierarchical)**
- **Low-Power Flow with Innovus Implementation System**
- **Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis**

**Equivalence Checking**
- **Basic Static Timing Analysis**
- **Tempus™ Signoff Timing Analysis and Closure**
- **Voltus™ Power-Grid Analysis and Signoff**
- **Conformal® Equivalence Checking**
- **Conformal Low-Power Verification**
- **Conformal ECO**

**Cadence® RTL-to-GDSII Flow**

- **New Course**
- **Number of days for instructor-led course**
- **Online Course Available**
- **Digital Badge Available**

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System Design and Verification Learning Map

**Design and Verification Languages**

- **Verilog Language and Application**
  - Master VHDL For Verilog Engineers
  - Real Modeling with Verilog AMS
  - Real Modeling with SystemVerilog
  - Perl for EDA Engineering
  - Tcl Scripting for EDA + Intro to Tk

- **SystemVerilog for Design and Verification**
  - Essential SystemVerilog for UVM (optional)
  - SystemVerilog Accelerated Verification Using UVM
  - SystemVerilog Advanced Register Verification Using UVM

- **UVM**

- **SystemVerilog Assertions**

- **VHDL Language and Application**
  - SystemVerilog for Design and Verification
  - SystemVerilog Assertions

- **C++ Language Fundamentals for Design and Verification**
  - SystemC® Language Fundamentals
  - SystemC Synthesis with Stratus HLS
  - SystemC Transaction-Level Modeling TLM2.0

- **JasperGold® Formal Fundamentals**

- **SVA, Formal & JasperGold® Fundamentals for Designers**

- **JasperGold® Formal Expert**

- **New Course**
  - Number of days for instructor-led course
  - Tiers of Cadence products used in course
  - Online Course Available
  - Digital Badge Available

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Tensilica Processor IP Learning Map

**Tensilica Xtensa LX**
- Processor Fundamentals
- Processor Interfaces
- Hardware Verification and EDA
- Instruction Extension Language and Design
- System Modeling using XTSC

**ConnX DSP**
- ConnX BBE16EP Baseband Engine
- ConnX BBE32EP Baseband Engine
- ConnX BBE64EP Baseband Engine

**Fusion DSP**
- Fusion F1 DSP
- Fusion G3 DSP
- Fusion G6 DSP

**HiFi Audio DSP**
- Audio Codec API
- HiFi 2/EP/Mini Audio Engine ISA
- HiFi 3 Audio Engine ISA
- HiFi 4 DSP
- HiFi 5 DSP

**Vision DSP**
- Vision P5 DSP
- Vision P6 DSP
- DNA 100 Architecture and Programming

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