Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- Allegro® Design Entry HDL Front-to-Back Flow
- Allegro Design Entry HDL Basics
- Allegro System Capture
- Allegro System Architect
- Allegro Design Reuse
- Allegro AMS Simulator

## PCB Design
- Allegro PCB Editor Basic Techniques
- Allegro PCB Editor Intermediate Techniques
- Allegro PCB Router Basics
- Allegro PCB Editor Advanced Methodologies
- Allegro High-Speed Constraint Management
- Allegro Update Training

## SI/PI Analysis
- Essential High-Speed PCB Design for Signal Integrity
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
- Allegro SigRity™ SI Foundations
- Allegro SigRity PI
- SigRity PowerDC™ and OptimizePI™
- SigRity Aurora
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM
- Clarity 3D Solver
- Celsius Thermal Solver

## Library Development
- Allegro PCB Librarian
- Allegro EDM PCB Librarian
- Allegro Design Entry HDL SKILL® Programming Language
- Allegro PCB Editor SKILL Programming Language

### New Course
- New Course

### Number of days for instructor-led course
- Number of days for instructor-led course

### Tiers of Cadence products used in course
- Tiers of Cadence products used in course

### Online Course Available
- Online Course Available

### Digital Badge Available
- Digital Badge Available

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Custom IC, Analog and RF Design Learning Map

IC CAD

SKILL Language Programming Introduction (New)
SKILL Language Programming
SKILL Development of Parameterized Cells
Advanced SKILL Language Programming

Layout Design and Advanced Nodes

Virtuoso® Layout Design Basics
Virtuoso Connectivity-Driven Layout Transition
Virtuoso Abstract Generator
Virtuoso Floorplanner
Virtuoso Simulation Driven Routing (SDR)

Virtuoso® Layout Pro Series

T1: Env. and Basic Commands
T2: Create and Edit Commands
T3: Basic Commands
T4: Advanced Commands
T5: Interactive Routing
T6: Constraint-Driven Flow and Power Routing
T7: Module Generator and Floorplanner
T8: Concurrent Layout Editing (Q3 2022)
T9: Virtuoso Design Planner

Virtuoso® Advanced-Node – ICADV

T1: Place and Route
T2: Electromigration

Virtuoso® Advanced-Node and Methodology - ICADVM

Virtuoso Layout for Advanced Nodes and Methodology Platform

Layout Verification

Pegasus Verification System (New)
Physical Verification System (PVS)
Physical Verification Language Rules-Writer

Quantus™ Extraction Solution Transistor-Level Series

T1: Overview and Technology Setup
T2: Parasitic Extraction
T3: Extracted View Flows and Advanced Features

New Course
Number of days for instructor-led course
Tiers of Cadence products used in course
Online Course Available
Digital Badge Available

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Digital Design and Signoff Learning Map

Synthesis and Test
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Stylus Common UI
  - Test Synthesis with Genus Stylus Common UI
  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

Implementation
- Innovus Implementation System (Block)
  - Innovus Implementation System (Hierarchical)
  - Low-Power Flow with Innovus Implementation System
  - Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

Silicon Signoff
- Basic Static Timing Analysis
- Tempus™ Sighnoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal Low-Power Verification Using IEEE1801
- Conformal ECO

Cadence® RTL-to-GDSII Flow

New Course
Number of days for instructor-led course
Online Course Available
Digital Badge Available