Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
### IC Package Design

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### SI/PI Analysis

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Custom IC, Analog and RF Design Learning Map

Circuit Design, Simulation, Modeling and RF Design

Virtuoso® Analog Design Environment

Virtuoso Analog Simulation Series

T1: Introduction to the Virtuoso ADE XL Environment
T2: Creating Sweeps and Running Corners
T3: Monte Carlo Simulation Using ADE XL
T4: Sensitivity Analysis and Circuit Optimization with ADE GXL

Mixed-Signal Simulations Using AMS Designer

Analog Modeling with Verilog-A

Behavioral Modeling with / Verilog-AMS / VHDL-AMS
Real Modeling with / SystemVerilog / Verilog-AMS
Transistor-Level Power Signoff with Voltus™-Fi

Virtuoso Schematic Editor

Virtuoso® ADE Explorer Series

S1: Set Up and Run Analog Simulations Using the Spectre® Simulator
S2: Analyzing Simulations Using ViVAX XL
S3: Corner Analysis and Monte Carlo Simulation
S4: Real-Time Tuning, Checks/Asserts, and Reliability Analysis

Virtuoso® ADE Assembler Series

S1: Introducing the Assembler Environment
S2: Sweeping Variables, Simulating Corners and Creating Run Plans
S3: Corner Analysis and Monte Carlo Simulation

Virtuoso ADE Assembler

Variation Analysis Using the Virtuoso ADE Assembler

Virtuoso Spectre Pro Series

S1: DC Algorithm
S2: AC, XF, STB, Noise
S3: Transient Algorithm
S4: Fourier Transform
S5: Transient Noise

Spectre® RF/Shooting Newton / Harmonic Balance

Spectre Simulator Fundamentals Series

S1: Spectre Basics
S2: Large-Signal
S3: Small-Signal
S4: Spectre MDL

High-Performance Simulation Using Spectre APS and XPS
Spectre APS
Virtuoso Electrically-Aware Design with LDE

Library Characterization

Cadence® Library Characterization and Validation
Virtuoso Liberate™ MX Memory Characterization
Cadence Variety™ Statistical Library Characterization

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# Digital Design and Signoff Learning Map

## Synthesis
- **Genus™ Synthesis Solution**
- **Low-Power Synthesis Flow with Genus Synthesis Solution**
- **Test Synthesis Using Genus Synthesis Solution**
- **Advanced Synthesis with Genus Synthesis Solution**
- **Fundamentals of IEEE 1801 Low-Power Specification Flow**
- **Modus Test Solution**
- **Joules™ Power Calculator**

## Implementation
- **Virtuoso® Digital Implementation**
- **Innovus™ Implementation System**
- **Innovus Implementation System (Hierarchical)**
- **Low-Power Flow with Innovus Implementation System**
- **Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis**
- **Analog-on-Top Mixed-Signal Implementation**

## Silicon Signoff
- **Basic Static Timing**
- **Tempus™ Signoff Timing Analysis and Closure**
- **Voltus™ Power-Grid Analysis and Signoff**

## Equivalence Checking
- **Logic Equivalence Checking with Conformal® EC**
- **Low-Power Verification with Conformal**
- **Conformal ECO**

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**Cadence® RTL-to-GDS Flow**

- **New Course**
- **Number of days for instructor-led course**
- **Online Course Available**

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# System Design and Verification Learning Map

## Simulation, Acceleration, Emulation, Coverage and Debug

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- New Course
- Number of days for instructor-led course
- L: Low, XL: Extra-Large, XXL: Extra-Extra-Large
- Tiers of Cadence products used in course
- Online Course Available

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