Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- **Beginner**
  - Allegro® Design Entry HDL Front-to-Back Flow
  - Allegro Design Entry HDL Basics
  - Allegro System Capture
- **Advanced**
  - Allegro AMS Simulator
  - Allegro Design Reuse
  - Allegro System Architect

## PCB Design
- **Beginner**
  - Allegro PCB Editor Basic Techniques
  - OrCAD Capture
  - OrCAD Capture Constraint Manager PCB Flow
- **Intermediate**
  - Allegro PCB Editor Intermediate Techniques
  - Allegro PCB Router Basics
  - Allegro Team Design Authoring
- **Advanced**
  - Allegro PCB Editor Advanced Methodologies
  - Allegro High-Speed Constraint Management
  - Analog Simulation with PSpice®

## SI/PI Analysis
- **Beginner**
  - Essential High-Speed PCB Design for Signal Integrity
  - PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
  - Allegro Sigrity™ SI Foundations
  - Allegro Sigrity PI
  - Sigtry PowerDC” and OptimizePI”
- **Advanced**
  - Sigtry Aurora
  - TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
  - Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM
  - Clarity 3D Solver
  - Celsius Thermal Solver

## Library Development
- **Beginner**
  - Allegro PCB Librarian
  - Allegro EDM PCB Librarian
- **Advanced**
  - Allegro Design Entry HDL SKILL® Programming Language
  - Allegro PCB Editor SKILL Programming Language
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New Course
New Number of days for instructor-led course
Tiers of Cadence products used in course
Online Course Available

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Custom IC, Analog and RF Design Learning Map

Circuit Design, Simulation, Modeling and RF Design

Analog Modeling with Verilog-A
Mixed-Signal Simulations using Spectre AMS Designer
Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model
Behavioral Modeling with Verilog AMS
Behavioral Modeling with VHDL-AMS
Real Modeling with Verilog-AMS
Real Modeling with SystemVerilog
SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

Virtuoso Schematic Editor
Virtuoso Visualization and Analysis
Virtuoso® ADE Explorer & Assembler Series
Virtuoso® ADE Verifier Series
Design Checks and Asserts

Spectre® Simulator Fundamentals Series
S1 Spectre Basics
S2 Large-Signal
S3 Small-Signal
S4 Spectre MDL

Spectre Accelerated Parallel Simulator (APS)
Spectre XPS for Mixed-Signal Designs

Virtuoso® Spectre® Pro Series
S1 DC Algorithm
S2 AC, XF, STB, Noise
S3 Transient Algorithm
S4 Fourier Transform
S5 Transient Noise

Spectre® RF Shooting Newton
Spectre® RF Harmonic Balance

5G mmWave Handset System Design – S1 RFIC (Transceiver) Design

New Course
Number of days for instructor-led course
Online Course Available
Digital Badge Available
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Digital Design and Signoff Learning Map

**Synthesis and Test**
- Design For Test Fundamentals
- Virtuoso® Digital Implementation
  - Genus™ Synthesis Solution with Stylus Common UI
  - Low-Power Synthesis Flow with Genus Stylus Common UI
  - Test Synthesis with Genus Stylus Common UI
  - Advanced Synthesis with Genus Stylus Common UI
  - Fundamentals of IEEE 1801 Low-Power Specification Format
  - Modus DFT Software Solution
  - Joules™ Power Calculator

**Implementation**
- Virtuoso® Digital Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

**Silicon Signoff**
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

**Equivalence Checking**
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO

Cadence® RTL-to-GDSII Flow
Tensilica Processor IP Learning Map

Tensilica Xtensa NX
- Processor Fundamentals
- Processor Interfaces
- Hardware Verification and EDA
- Instruction Extension Language and Design
- System Modeling using XTSC

ConnX DSP
- ConnX B10 DSP
- ConnX B20 DSP

Vision DSP
- Vision Q7 DSP

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