Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents
• PCB Design and Analysis
• Custom IC, Analog, and RF Design
• Digital Design and Signoff
• System Design and Analysis
• IC Package Design and Analysis
• Tensilica® Processor IP
PCB Design and Analysis Learning Map

**Logic Design**
- Allegro® Design Entry HDL Front-to-Back Flow
- Allegro Design Entry HDL Basics
- Allegro System Capture
- Allegro System Architect
- Allegro Design Reuse
- Allegro AMS Simulator
  - Allegro AMS Simulator Advanced Analysis
- Allegro Design Entry Using OrCAD® Capture
- OrCAD CIS
- OrCAD Capture Constraint Manager PCB Flow
- Allegro EDM Design Entry HDL Front-to-Back Flow
- Allegro Team Design Authoring
- Analog Simulation with PSpice®

**PCB Design**
- Allegro PCB Editor Basic Techniques
  - Allegro PCB Editor Intermediate Techniques
  - Allegro PCB Router Basics
  - Allegro PCB Editor Advanced Methodologies
- Allegro High-Speed Constraint Management
- Advanced Design Verification with the RAVEI Programming Language

**SI/PI Analysis**
- Essential High-Speed PCB Design for Signal Integrity
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
- Allegro Sigtry™ SI Foundations
- Allegro Sigtry PI
- Sigtry PowerDC™ and OptimizePI™
- Sigtry Aurora
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM
- Clarity 3D Solver
- Celsius Thermal Solver

**Library Development**
- Allegro PCB Librarian
- Allegro EDM PCB Librarian
- Allegro Design Entry HDL SKILL® Programming Language
- Allegro PCB Editor SKILL Programming Language

© 2020 Cadence Design Systems, Inc.
<table>
<thead>
<tr>
<th>IC Package Design</th>
<th>SI/PI Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td>Allegro Sigrity™ SI Foundations</td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td>Allegro Sigrity PI</td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td>Sigrity PowerDC™ and OptimizePI™</td>
</tr>
<tr>
<td>Allegro Sigrity Package Assessment and Model Extraction</td>
<td>TopXplorer SystemSI for Parallel Bus and Serial Link Analysis</td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td>Clarity 3D Solver</td>
</tr>
<tr>
<td>Allegro Package Designer Plus</td>
<td>Celsius Thermal Solver</td>
</tr>
</tbody>
</table>

New Course  
Number of days for instructor-led course  
Tiers of Cadence products used in course  
Online Course Available  
© 2020 Cadence Design Systems, Inc.
Custom IC, Analog and RF Design Learning Map

Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

Mixed-Signal Simulation
- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model
- SimVision for Debugging Mixed-Signal Simulations

AMS/Real Number Modeling
- Analog Modeling with Verilog-A
- Behavioral Modeling with Verilog AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

Virtuoso® ADE Explorer & Assembler Series
- S1 ADE Explorer & Single Test Corner Analysis
- S2 ADE Assembler & Multi Test Corner Analysis
- S3 Sweeping Variables and Simulating Corners
- S4 Monte Carlo, Real-Time Tuning & Run Plans

Virtuoso® ADE Verifier Series
- S1 Setup, Run, & View Verifier Results
- S2 Reference Flow and Analog Coverage Using the Setup Library Assistant
- 5G mmWave Handset System Design – S1 RFIC (Transceiver) Design

Virtuoso Visualization and Analysis

Spectre® Simulator Fundamentals Series
- S1 Spectre Basics
- S2 Large-Signal Analysis
- S3 Small-Signal Analysis
- S4 Spectre MDL

High Performance Spectre Simulation
- Virtuoso® Spectre® Pro Series
- S1 DC Algorithm
- S2 AC, XF, STB, Noise
- S3 Transient Algorithm
- S4 Fourier Transform
- S5 Transient Noise

Spectre RF Series
- Spectre® RF Shooting Newton
- Spectre® RF Harmonic Balance

Mixed-Signal Simulation

Behavioral Modeling with Verilog AMS

Real Modeling with SystemVerilog

SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification

5G mmWave Handset System Design – S1 RFIC (Transceiver) Design

© 2020 Cadence Design Systems, Inc.
System Design and Verification Learning Map

**Design and Verification Languages**

- **Verilog Language and Application**
  - Real Modeling with Verilog
  - Real Modeling with SystemVerilog
  - SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
  - Perl for EDA Engineering
  - Tcl Scripting for EDA

- **SystemVerilog for Design and Verification**
  - SystemVerilog for Design and Verification

- **UVM**
  - Essential SystemVerilog for UVM (optional)
  - SystemVerilog Accelerated Verification Using UVM

- **SystemVerilog Advanced Register Verification Using UVM**

- **SystemVerilog Assertions**

- **JasperGold® Formal Fundamentals**

- **JasperGold® Formal Expert**

- **VHDL Language and Application**

- **C++ Language Fundamentals for Design and Verification**

- **SystemC® Language Fundamentals**

- **SystemC Synthesis with Stratus HLS**

- **SystemC Transaction-Level Modeling TLM2.0**

- **SystemVerilog Accelerated Verification Using UVM**

- **SystemVerilog for Design and Verification**

- **SystemVerilog for Design and Verification**

- **SystemVerilog Assertions**

- **JasperGold® Formal Fundamentals for Designers**

- **JasperGold® Formal Expert**

- **Perl for EDA Engineering**

- **Tcl Scripting for EDA**

**New Course**
- Number of days for instructor-led course
- Tiers of Cadence products used in course
- Online Course Available
- Digital Badge Available

© 2020 Cadence Design Systems, Inc.
Tensilica Processor IP Learning Map

**Tensilica Xtensa® NX**
- Processor Fundamentals
- Xtensa NX Processor Interfaces
- Instruction Extension Language and Design
- System Modeling using XTSC

**ConnX DSP**
- ConnX B10 DSP
- ConnX B20 DSP

**Vision DSP**
- Tensilica Vision DSP Family
- Tensilica Xtensa Neural Network Compiler v2