Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

**Contents**

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

<table>
<thead>
<tr>
<th>Logic Design</th>
<th>PCB Design</th>
<th>SI/PI Analysis</th>
<th>Library Development</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Beginner</strong></td>
<td><strong>Beginner</strong></td>
<td><strong>Beginner</strong></td>
<td><strong>Beginner</strong></td>
</tr>
<tr>
<td>Allegro® Design Entry HDL Front-to-Back Flow</td>
<td>Allegro Design Entry Using OrCAD® Capture</td>
<td>Essential High-Speed PCB Design for Signal Integrity</td>
<td>Allegro PCB Librarian</td>
</tr>
<tr>
<td>Allegro Design Entry HDL Basics</td>
<td>OrCAD CIS</td>
<td>PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials</td>
<td>Allegro EDM PCB Librarian</td>
</tr>
<tr>
<td>Allegro System Design Authoring</td>
<td>Allegro EDM Design Entry HDL Front-to-Back Flow</td>
<td>Allegro Sigry™ SI Foundations</td>
<td>Allegro EDM for Administrators</td>
</tr>
<tr>
<td>Allegro System Architect</td>
<td>Allegro Team Design Authoring</td>
<td>Allegro Sigry PI</td>
<td>Allegro EDM Administration for OrCAD</td>
</tr>
<tr>
<td>Allegro Design Reuse</td>
<td>Allegro EDM for Engineers and Designers</td>
<td>Sigry PowerDC™ and OptimizePI™</td>
<td>Allegro Design Entry HDL SKILL® Programming Language</td>
</tr>
<tr>
<td>Allegro AMS Simulator</td>
<td>Analog Simulation with PSpice®</td>
<td>Allegro Update Training</td>
<td>Allegro PCB Editor SKILL Programming Language</td>
</tr>
<tr>
<td>Allegro AMS Simulator Advanced Analysis</td>
<td>Allegro Simulation with PSpice Advanced Analysis</td>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td>Advanced Design Verification using PowerSI, Broadband SPICE and 3D-EM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### IC Package Design

<table>
<thead>
<tr>
<th>Course</th>
<th>Number of days</th>
<th>Tiers of Cadence products used in course</th>
<th>Online Course Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP Layout</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro® Package Designer</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro FPGA System Planner</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro Sigtry Package Assessment and Model Extraction</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OrbitIO™ System Planner</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advanced Design Verification with the RAVEL Programming Language</td>
<td>2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SI/PI Analysis

<table>
<thead>
<tr>
<th>Course</th>
<th>Number of days</th>
<th>Tiers of Cadence products used in course</th>
<th>Online Course Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allegro Sigtry™ SI Foundations</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro Sigtry PI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sigtry PowerDC™ and OptimizePI™</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sigtry SystemSI™ for Parallel Bus and Serial Link Analysis</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Custom IC, Analog and RF Design Learning Map

Virtuoso Schematic Editor

IC 6.1.7 Virtuoso® ADE Explorer Series

S1 Set Up and Run Analog Simulations
S2 Analyzing Simulations Using the ViVA XL Waveform Tool
S3 Corner Analysis & Monte Carlo Simulations
S4 Real-Time Tuning, Checks /Asserts, Reliability Analysis

IC 6.1.7 Virtuoso® ADE Assembler Series

S1 Introducing the Assembler Environment
S2 Sweeping Variables, Simulating Corners & Creating Run Plans
S3 Circuit Checks, Device Asserts and Reliability Analysis

Mixed-Signal Simulations using Spectre AMS Designer
Command-Line Based Mixed-Signal Simulations w/ Xcellium Use Model
Mixed-Signal IP & Testbench Reuse

Virtuoso Visualization and Analysis XL

IC 6.1.8 Virtuoso® ADE Explorer & Assembler Series

S1 ADE Explorer & Single Test Corner Analysis
S2 ADE Assembler & Multi Test Corner Analysis
S3 Sweeping Variables and Simulating Corners
S4 Monte Carlo, Real-Time Tuning & Run Plans

Design Checks and Asserts

Virtuoso® ADE Verifier Series

S1 Setup, Run, View Verif. Results
S2 Reference Flow and Analog Coverage Using the Setup Library Assistant

Variation Analysis using the Variation Option

Analog Modeling with Verilog-A
Behavioral Modeling w/ Verilog AMS
Behavioral Modeling with VHDL-AMS
Real Modeling with SystemVerilog
Real Modeling with Verilog-AMS
Transistor Power Signoff w/ Voltus™-Fi

Virtuoso Spectre Pro Series

S1 DC Algorithm
S2 AC, XF, STB, Noise
S3 Transient Algorithm
S4 Fourier Transform
S5 Transient Noise

Spectre® RF Shooting Newton
Spectre® RF Harmonic Balance

Virtuoso Spectre Simulator Fundamentals Series

S1 Spectre Basics
S2 Large-Signal
S3 Small-Signal
S4 Spectre MDL

Spectre Accelerated Parallel Simulator (APS)
Spectre XPS for Mixed-Signal Designs
Virtuoso EAD with LDE

Virtuoso Analog Design Environment

Virtuoso® Analog Simulation Series

T1 Xcelium
T2 Virtuoso Visualization and Analysis XL
T3 XL
T4 XL

Library Characterization

Liberate™ Characterization Portfolio
Liberate™ MX Memory Characterization
Liberate™ Variety™ Statistical Library Characterization

Tiers of Cadence products used in course
Online Course Available
Digital Badge Available
© 2019 Cadence Design Systems, Inc.
Custom IC, Analog and RF Design Learning Map

**IC CAD**
- **SKILL Language Programming**
  - Introduction
  - Fundamentals
- **SKILL Programming for Layout Design**
- **SKILL Development of Parameterized Cells**
- **Advanced SKILL Language Programming**

**Layout Design and Advanced Nodes**
- **Virtuoso® Layout Design Basics**
- **Virtuoso Connectivity-Driven Layout Transition**
- **Virtuoso Abstract Generator**
- **Virtuoso Floorplanner**
- **Virtuoso Space-Based Router**
- **Virtuoso Space-Based Router Express**
- **Virtuoso® Advanced-Node Series – ICADV**
  - **T1: Place and Route**
  - **T2: Electromigration**

**Virtuoso® Layout Pro Series**
- **T1: Env. and Basic Commands**
- **T2: Create and Edit Commands**
- **T3: Basic Commands**
- **T4: Advanced Commands**
- **T5: Interactive Routing**
- **T6: Constraint-Driven Flow and Power Routing**
- **T7: Module Generator and Floorplanner**
- **T8: Debugging Layout Issues**

**Virtuoso® Layout Pro Series – ICADV**
- **T1: Place and Route**
- **T2: Electromigration**

**Physical Verification System (PVS)**
- **Physical Verification Language Rules-Writer**

**Quantus™ Extraction Solution**
- **Transistor-Level Series**
- **Physical Verification System (PVS)**
- **T1: Overview and Technology Setup**
- **T2: Parasitic Extraction**
- **T3: Extracted View Flows and Advanced Features**

---

© 2019 Cadence Design Systems, Inc.
Digital Design and Signoff Learning Map

### Synthesis and Test
- Design For Test Fundamentals
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Synthesis Solution
- Test Synthesis Using Genus Synthesis Solution
- Advanced Synthesis with Genus Stylus Common UI

### Implementation
- Virtuoso® Digital Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis
- Analog-on-Top Mixed-Signal Implementation

### Silicon Signoff
- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

### Equivalence Checking
- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO
- Conformal Constraint Designer
System Design and Verification Learning Map

Simulation, Acceleration, Coverage and Debug

Incisive® SystemC®, VHDL, and Verilog Simulation
- Incisive Comprehensive Coverage with IMC
- Incisive Simulation Performance Optimization
- Perspec™ System Verifier - Basic
- Low-Power Simulation with CPF
- Low-Power Simulation with IEEE1801 UPF
- Incisive Functional Safety Simulator

Xcelium™ Simulator
- Cadence® RTL-To-GDSII Flow
- Foundations of Metric-Driven Verification
- Xcelium Integrated Coverage
- Indago™ Debug Analyzer App
- Metric-Driven Verification Using vManager™
- vManager Tool Usage in Batch Mode

Specman® New Fundamentals for Block-level Environment Developers
- Specman Advanced Verification
- VIP Basic Building Blocks and Usage

New Course
Number of days for instructor-led course
Tiers of Cadence products used in course
Online Course Available
© 2019 Cadence Design Systems, Inc.
System Design and Verification Learning Map

Design and Verification Languages

- Verilog Language and Application
  - Master VHDL For Verilog Engineers
    - SystemVerilog Advanced / Accelerated Verification Using UVM
      - SystemVerilog Advanced Register Verification Using UVM
  - Verilog for VHDL Users
    - SystemVerilog Assertions
      - JasperGold® Formal Fundamentals
- VHDL Language and Application
  - Verification with PSL
    - SystemC Transaction-Level Modeling TLM2.0
      - Perl for EDA Engineering
      - Tcl Scripting for EDA + Intro to Tk
  - SystemC® Language Fundamentals
    - SystemC Synthesis with Stratus HLS
      - Perl for EDA Engineering
      - Tcl Scripting for EDA + Intro to Tk
- C++ Language Fundamentals for Design and Verification
  - SystemC® Language Fundamentals
    - SystemC Synthesis with Stratus HLS
      - Perl for EDA Engineering
      - Tcl Scripting for EDA + Intro to Tk

Advanced

Beginner

New Course
Number of days for instructor-led course
Tiers of Cadence products used in course
Online Course Available
© 2019 Cadence Design Systems, Inc.