



# Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

## Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

# PCB Design and Analysis Learning Map

Beginner

Advanced

Beginner

Advanced



# IC Package Design and Analysis Learning Map

Beginner



Advanced

## IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



Allegro Package Designer Plus **NEW**



## SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis



Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM



Clarity 3D Solver **NEW**



Celsius Thermal Solver **NEW**



Beginner



Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

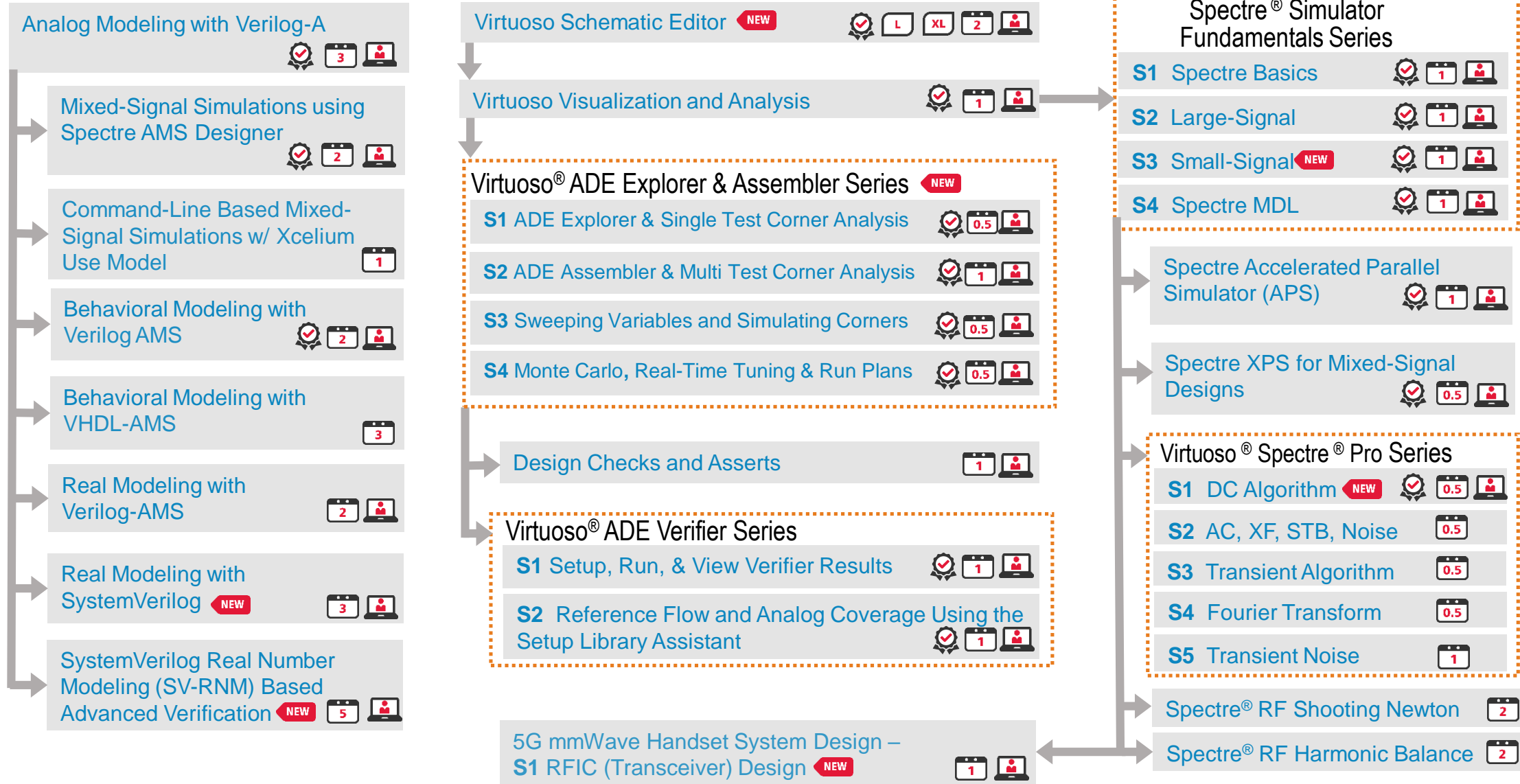
Beginner

Advanced

Beginner

Advanced

## Circuit Design, Simulation, Modeling and RF Design



Beginner

Advanced

Beginner

Advanced

## IC CAD

- SKILL® Language Programming Introduction 2 NEW
- SKILL Language Programming 5
- SKILL Development of Parameterized Cells 2
- Advanced SKILL Language Programming 3

## Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics 1
- Virtuoso Connectivity-Driven Layout Transition 2
- Virtuoso Abstract Generator 1
- Virtuoso Floorplanner 1
- Virtuoso Space-Based Router 2
- Virtuoso Space-Based Router Express 0.5
- Virtuoso Simulation Driven Routing (SDR) 0.5 NEW

### Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands 1
- T2: Create and Edit Commands 1
- T3: Basic Commands 1
- T4: Advanced Commands 1
- T5: Interactive Routing 1
- T6: Constraint-Driven Flow and Power Routing 1 NEW
- T7: Module Generator and Floorplanner 0.5
- T8: Debugging Layout Issues 0.5
- T9: Virtuoso Design Planner 2

- Virtuoso® Advanced-Node – ICADV
  - Virtuoso Layout for Adv. Nodes 2
  - T1: Place and Route 1
  - T2: Electromigration 0.5
- Virtuoso® Advanced-Node and Methodology - ICADV
  - Virtuoso Layout for Advanced Nodes and Methodology Platform 0.5 NEW

## Layout Verification

- Pegasus Verification System 2 NEW
- Physical Verification System (PVS) 2
- Physical Verification Language Rules-Writer 2
- Quantus™ Extraction Solution Transistor-Level Series
  - T1: Overview and Technology Setup 0.5
  - T2: Parasitic Extraction 1
  - T3: Extracted View Flows and Advanced Features 0.5

# Digital Design and Signoff Learning Map

Beginner

Advanced

Beginner

Advanced

## Synthesis and Test      Implementation      Silicon Signoff      Equivalence Checking

Cadence® RTL-to-GDSII Flow



Design For Test Fundamentals



Virtuoso® Digital Implementation



Genus™ Synthesis Solution with Stylus Common UI



Low-Power Synthesis Flow with Genus Stylus Common UI



NEW

Test Synthesis with Genus Stylus Common UI



NEW

Advanced Synthesis with Genus Stylus Common UI



Fundamentals of IEEE 1801 Low-Power Specification Format



Modus DFT Software Solution



Joules™ Power Calculator



Innovus™ Implementation System (Block)



Innovus Implementation System (Hierarchical)



Low-Power Flow with Innovus Implementation System



Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis



Basic Static Timing Analysis



Tempus™ Signoff Timing Analysis and Closure



Voltus™ Power-Grid Analysis and Signoff



Conformal® Equivalence Checking



Conformal Low-Power Verification



Conformal ECO

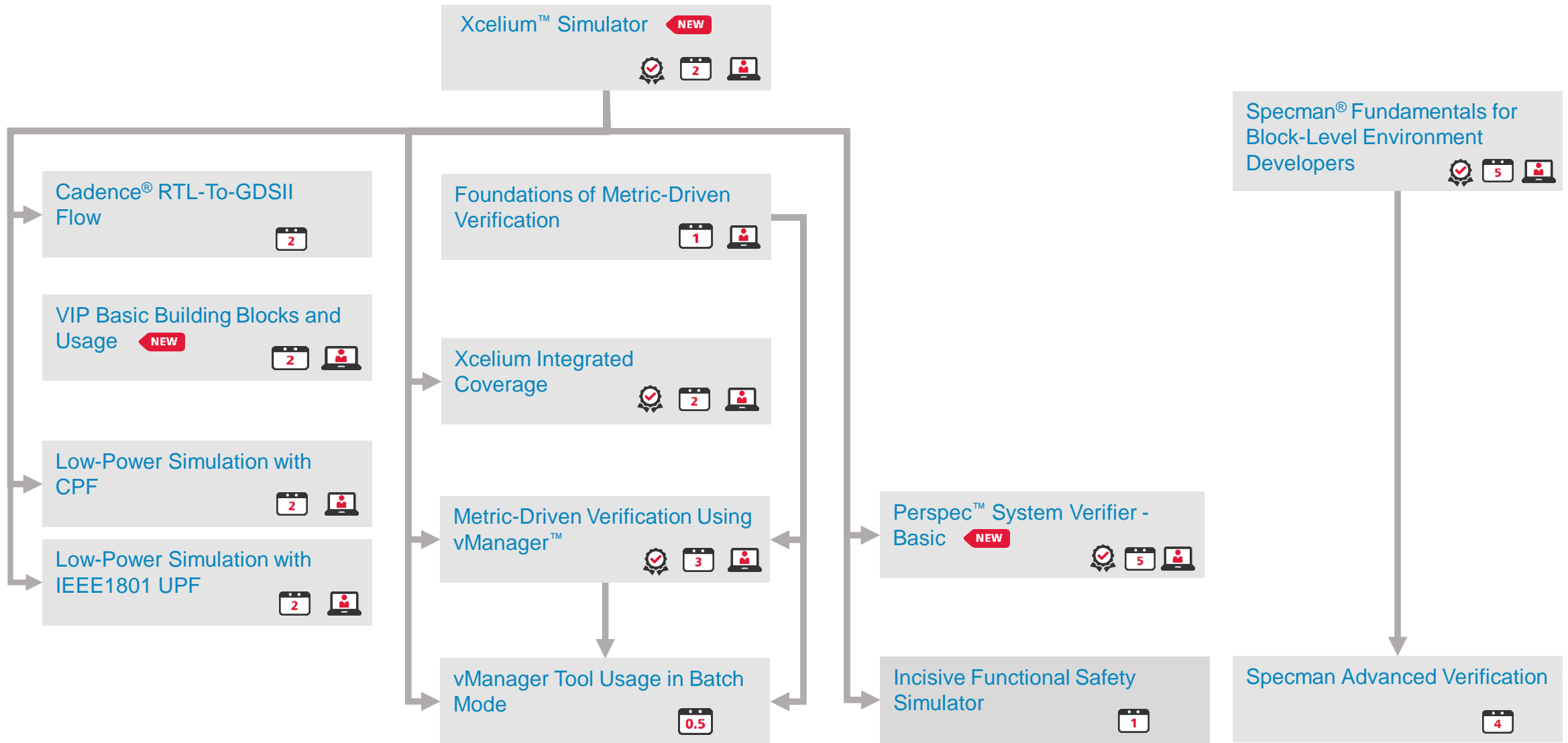


# System Design and Verification Learning Map

Beginner

Beginner

## Simulation, Coverage and Debug



Advanced

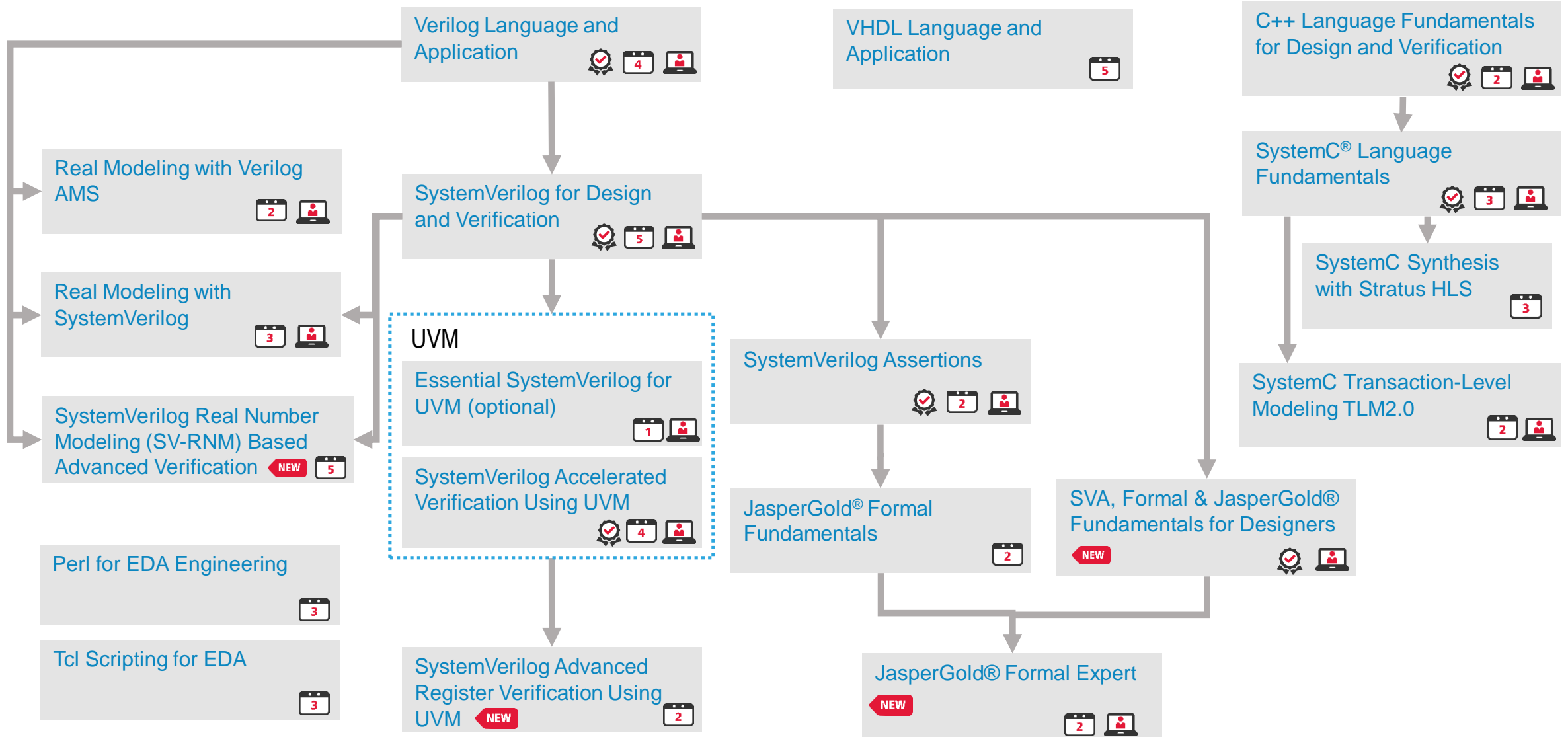
Advanced

# System Design and Verification Learning Map

Beginner

Beginner

## Design and Verification Languages



Advanced

Advanced



# Tensilica Processor IP Learning Map



## Tensilica Xtensa LX

## ConnX DSP

## Fusion DSP

## HiFi Audio DSP

## Vision DSP

[Tensilica® Xtensa® LX Processor Fundamentals](#)

NEW



[Tensilica Xtensa LX Processor Interfaces](#)



[Tensilica Xtensa LX Hardware Verification and EDA](#)



[Tensilica Instruction Extension Language and Design](#)

1



[Tensilica System Modeling using XTSC](#)

NEW



[Tensilica ConnX BBE16EP Baseband Engine](#)

2

[Tensilica ConnX BBE32EP Baseband Engine](#)

2



[Tensilica ConnX BBE64EP Baseband Engine](#)

2

[Tensilica Fusion F1 DSP](#)



[Tensilica Fusion G3 DSP](#)

2



[Tensilica Fusion G6 DSP](#)

2

[Tensilica Audio Codec API](#)

0.5

[Tensilica HiFi 2/EP/Mini Audio Engine ISA](#)



[Tensilica HiFi 3 Audio Engine ISA](#)



[Tensilica HiFi 4 DSP](#)

NEW



[Tensilica HiFi 5 DSP](#)

NEW



[Tensilica Vision P5 DSP](#)

2



[Tensilica Vision P6 DSP](#)

2



[Tensilica DNA 100 Architecture and Programming](#)

NEW



NEW

New Course



Number of days for instructor-led course





Online Course Available

# Tensilica Processor IP Learning Map


## Tensilica Xtensa NX



## ConnX DSP



## Vision DSP




[Tensilica® Xtensa® NX Processor Fundamentals](#)  



[Tensilica Xtensa NX Processor Interfaces](#) 



[Tensilica Xtensa NX Hardware Verification and EDA](#) 

[Tensilica Instruction Extension Language and Design](#)  

[Tensilica System Modeling using XTSC](#)  

[Tensilica ConnX B10 DSP](#)   

[Tensilica ConnX B20 DSP](#)  

[Tensilica Vision Q7 DSP](#)  



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