Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® Technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

PCB Design and Analysis Learning Map

Beginner

Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow
- Allegro Design Entry HDL Basics
- Allegro System Design Authoring NEW
- Allegro System Architect
- Allegro Design Reuse
- Allegro AMS Simulator
  - Allegro AMS Simulator Advanced Analysis
- Allegro Design Entry Using OrCAD® Capture
- OrCAD CIS
- Allegro EDM Design Entry HDL Front-to-Back Flow NEW
- Allegro Team Design Authoring
- Allegro EDM for Engineers and Designers
- Analog Simulation with PSpice®
  - Analog Simulation with PSpice Advanced Analysis

PCB Design

- Allegro PCB Editor Basic Techniques
  - Allegro PCB Editor Intermediate Techniques
  - Allegro PCB Router Basics
  - Allegro PCB Editor Advanced Methodologies NEW
- Allegro High-Speed Constraint Management
- Allegro Update Training NEW
- Advanced Design Verification with the RAVEL Programming Language NEW

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials
- Allegro Sigrity™ SI Foundations
- Allegro Sigrity PI
- Sigrity PowerDC™ and OptimizePI™
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis NEW
- Sigrity PowerSI® for Model Generation and Analysis

Library Development

- Allegro PCB Librarian
- Allegro Design Workbench for Librarians
- Allegro Design Workbench for Administrators
- Allegro Design Entry HDL SKILL® Programming Language
- Allegro PCB Editor SKILL Programming Language
- Allegro Tool Setup and Configuration

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout — 5 days
- Allegro® Package Designer — 4 days
- Allegro FPGA System Planner — 2 days
- Allegro Sigrity Package Assessment and Model Extraction — 1 day
- OrbitIO™ System Planner — 1 day
- Advanced Design Verification with the RAVEL Programming Language NEW — 2 days

SI/PI Analysis

- Allegro Sigrity™ SI Foundations — 2 days
- Allegro Sigrity PI — 1 day
- Sigrity PowerDC™ and OptimizePI™ — 1 day
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis NEW — 3 days
- Sigrity PowerSI® for Model Generation and Analysis — 2 days

Beginner

Advanced

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

Virtuoso® Analog Design Environment

L 3

Virtuoso Analog Simulation Series

- **T1** The Virtuoso Analog Design XL Environment — XL 1
- **T2** Creating Sweeps and Running Corner Analysis — XL 0.5
- **T3** Monte Carlo Simulation Using ADE XL — XL 0.5
- **T4** Sensitivity Analysis and Circuit Optimization Using ADE GXL — GXL 0.5

Mixed-Signal Simulations using Spectre AMS Designer NEW — 2

Mixed-Signal IP & Testbench Reuse — 0.5 NEW

Analog Modeling with Verilog-A — 3

- Behavioral Modeling with / Verilog-AMS — 2 / VHDL-AMS — 3
- Real Modeling with / SystemVerilog / Verilog-AMS — 2
- Transistor-Level Power Signoff with Voltus™-Fi — 1.5

Virtuoso Schematic Editor

L XL 2

Virtuoso® ADE Explorer Series

- **S1** Set Up and Run Analog Simulations Using the Spectre® Simulator — 0.5
- **S2** Analyzing Simulations Using the ViVA XL Waveform Tool — 0.5
- **S3** Corner Analysis and Monte Carlo Simulations — 0.5
- **S4** Real-Time Tuning, Checks/Asserts, and Reliability Analysis — 0.5

Virtuoso ADE Assembler Series

- **S1** Introducing the Assembler Environment — 0.5
- **S2** Sweeping Variables, Simulating Corners and Creating Run Plans — 0.5
- **S3** Circuit Checks, Device Asserts and Reliability Analysis — 0.5

Virtuoso ADE Verifier — 1

Variation Analysis Using the Virtuoso Variation Option — 1

Spectre Simulator Fundamentals Series

- **S1** Spectre Basics — 0.5
- **S2** Large-Signal — 0.5
- **S3** Small-Signal — 0.5
- **S4** Spectre MDL — 0.5

Design Checks & Asserts NEW — 1

Spectre Accelerated Parallel Simulator (APS) NEW — 1

Spectre XPS for Mixed-Signal Designs NEW — 1

Virtuoso EAD with LDE — 1

Virtuoso Spectre Pro Series

- **S1** DC Algorithm — 0.5
- **S2** AC, XF, STB, Noise — 0.5
- **S3** Transient Algorithm — 0.5
- **S4** Fourier Transform — 0.5
- **S5** Transient Noise — 1

Spectre® RF/ Shooting Newton / Harmonic Balance — 2

Library Characterization

Cadence® Library Characterization and Validation — 2

Virtuoso Liberate™ MX for Memory Characterization — 2.5

Cadence Variety™ Statistical Library Characterization — 1

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Custom IC, Analog and RF Design Learning Map

2 of 2 – see prior page

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2 days, Online
- SKILL Language Programming Fundamentals — 3 days
- SKILL Language Programming — Digital Badge, 5 days, Online
- SKILL Development of Parameterized Cells — 2 days, Online
- SKILL Programming for IC Layout Design — 2 days
- Advanced SKILL Language Programming — 3 days, Online

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics — L, 1 day, Online
- Virtuoso Connectivity-Driven Layout Transition — Digital Badge, L, XL, 2 days, Online
  - Virtuoso Abstract Generator — NEW, GXL, 1 day, Online
  - Virtuoso Floorplanner — GXL, 1 day, Online
  - Virtuoso Space-Based Router — GXL, 2 days, Online
    - Virtuoso Space-Based Router Express — NEW, GXL, 0.5 day, Online

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — Digital Badge, L, 0.5 day, Online
- T2: Create and Edit Commands — Digital Badge, L, 0.5 day, Online
- T3: Basic Commands — XL, 0.5 day, Online
- T4: Advanced Commands — XL, 0.5 day, Online
- T5: Interactive Routing — XL, 0.5 day, Online
- T6: Constraint-Driven Flow and Power Routing — XL, GXL, 0.5 day, Online
- T7: Module Generator and Floorplanner — XL, GXL, 0.5 day, Online
- T8: Debugging Layout Issues — L, XL, 0.5 day, Online

Virtuoso® Advanced-Node Series – ICADV

- Virtuoso Layout for Advanced Nodes — 2 days, Online
- T1: Place and Route — NEW, Digital Badge, 1 day, Online
- T2: Electromigration — NEW, Digital Badge, 0.5 day, Online

Layout Verification

- Physical Verification System (PVS) — 2 days, Online
  - Physical Verification Language Rules-Writer — 2 days

Quantus™ QRC Transistor-Level Series — NEW

- T1: Overview and Technology Setup — 0.5 day, Online
- T2: Parasitic Extraction — 1 day, Online
- T3: Extracted View Flows and Advanced Features — 0.5 day, Online

- Assura® Verification DRC/LVS — 2 days
  - Assura Rules-Writer — 4 days

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis

- Genus™ Synthesis Solution — 2
- Low-Power Synthesis Flow with Genus Synthesis Solution — 1
- Test Synthesis Using Genus Synthesis Solution — 2
- Advanced Synthesis with Genus Synthesis Solution — 1
- Fundamentals of IEEE 1801 Low-Power Specification Format — 1
- Modus DFT Software Solution — 1
- Joules™ Power Calculator — 2

Implementation

- Virtuoso® Digital Implementation — 2
- Innovus™ Implementation System (Block) — 3
- Innovus Implementation System (Hierarchical) — 1
- Low-Power Flow with Innovus Implementation System — 1
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis — 1
- Analog-on-Top Mixed-Signal Implementation — 2

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure — 2
- Voltus™ Power-Grid Analysis and Signoff — 2

Equivalence Checking

- Conformal® Equivalence Checking — 2
- Conformal Low-Power Verification — 1
- Conformal ECO — 1
- Conformal Constraint Designer — 1

Cadence® RTL-to-GDS Flow — 2

NEW New Course

Number of days for instructor-led course

Online Course Available

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Acceleration, Coverage and Debug

- Incisive® SystemC®, VHDL, and Verilog Simulation — 2 — Online
- Incisive Comprehensive Coverage with IMC — 2 — Online
- Incisive Simulation Performance Optimization — NEW — Online
- Perspec™ System Verifier — Online
- Indago™ Analyzer App (15.2) — Online
- Low-Power Simulation with CPF — 2 — Online
- Low-Power Simulation with IEEE1801 UPF — 2 — Online
- Incisive Functional Safety Simulator — NEW — 1
- Xcelium™ Simulator — NEW — 2 — Online
- Cadence® RTL-To-GDSII Flow — NEW — 2
- Foundations of Metric-Driven Verification — 1 — Online
- Xcelium Integrated Coverage — NEW — 2 — Online
- Indago Analyzer App (17.10) — NEW — Online
- Metric-Driven Verification Using vManager™ — NEW — 3 — Online
- vManager Tool Usage in Batch Mode — 0.5
- Specman® Fundamentals for Block-level Environment Developers — 5 — Online
- Specman Advanced Verification — 4
- VIP Basic Building Blocks and Usage — NEW — 2 — Online

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application (4)
  - Master VHDL For Verilog Engineers (3)
  - SystemVerilog for Design and Verification (5)
    - SystemVerilog Advanced / Accelerated Verification Using UVM (5)
      - SystemVerilog Advanced Register Verification Using UVM NEW (2)
  - Real Modeling with Verilog AMS (2)
    - Real Modeling with SystemVerilog AMS NEW (2)
- VHDL Language and Application (5)
  - Verilog for VHDL Users (2)
  - SystemVerilog Assertions (2)
    - JasperGold® Formal Fundamentals NEW (3)
  - Verification with PSL (2)
- C++ Language Fundamentals for Design and Verification (2)
  - SystemC® Language Fundamentals (3)
    - SystemC Synthesis with Stratus HLS NEW (3)
    - SystemC Transaction-Level Modeling TLM2.0 (2)
  - Perl for EDA Engineering (3)
  - Tcl Scripting for EDA + Intro to Tk (3)

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Tensilica Processor IP Learning Map

Tensilica Processors

- Tensilica® Processor Fundamentals — 2 days, Online Course Available
- Tensilica Xtensa® Processor Interfaces — Online Course Available
- Tensilica Xtensa Hardware Verification and EDA — Online Course Available
- Tensilica Instruction Extension Language and Design — 1 day, Online Course Available
- Introduction to System Modeling with Tensilica Processor Cores — 1 day, Online Course Available

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine — 2 days, Online Course Available
- Tensilica ConnX BBE32EP Baseband Engine — 2 days, Online Course Available
- Tensilica ConnX BBE64EP Baseband Engine — 2 days, Online Course Available

Fusion DSP

- Tensilica Fusion F1 DSP — Online Course Available
- Tensilica Fusion G3 DSP — 2 days, Online Course Available
- Tensilica Fusion G6 DSP — 2 days, Online Course Available

HiFi Audio DSP

- Tensilica Audio Codec API — 0.5 days, Online Course Available
- Tensilica HiFi 2/EP/Mini Audio Engine ISA — Online Course Available
- Tensilica HiFi 3 Audio Engine ISA — 1 day, Online Course Available
- Tensilica HiFi 4 DSP — NEW — 1 day

Vision DSP

- Tensilica Vision P5 DSP — 2 days, Online Course Available
- Tensilica Vision P6 DSP — 2 days, Online Course Available
- Tensilica Vision C5 DSP — NEW — 1 day, Online Course Available

NEW New Course | # Number of days for instructor-led course | Online Course Available