Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

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- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
# PCB Design and Analysis Learning Map

## Logic Design
- **Allegro® Design Entry HDL Front-to-Back Flow**
- **Allegro Design Entry Using OrCAD® Capture**
- **OrCAD CIS**
- **OrCAD Capture Constraint Manager PCB Flow**
- **Allegro System Architect**
- **Allegro Design Reuse**
- **Allegro AMS Simulator**
- **Allegro AMS Simulator Advanced Analysis**

## PCB Design
- **Allegro PCB Editor Basic Techniques**
- **Allegro PCB Editor Intermediate Techniques**
- **Allegro PCB Router Basics**
- **Allegro PCB Editor Advanced Methodologies**
- **Allegro High-Speed Constraint Management**
- **Allegro Update Training**
- **Advanced Design Verification with the RAVEL Programming Language**

## SI/PI Analysis
- **Essential High-Speed PCB Design for Signal Integrity**
- **PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials**
- **Allegro Sigtry™ SI Foundations**
- **Allegro Sigtry PI**
- **Sigrity PowerDC™ and OptimizePI™**
- **TopXplorer SystemSI for Parallel Bus and Serial Link Analysis**
- **Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM**
- **Clarity 3D Solver**
- **Celsius Thermal Solver**

## Library Development
- **Allegro PCB Librarian**
- **Allegro EDM PCB Librarian**
- **Allegro EDM for Administrators**
- **Allegro EDM Administration for OrCAD**
- **Allegro Design Entry HDL SKILL® Programming Language**
- **Allegro PCB Editor SKILL Programming Language**

### Course Information
- **New Course**
- **Number of days for instructor-led course**
- **Tiers of Cadence products used in course**
- **Online Course Available**
- **Digital Badge Available**

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<td><strong>Allegro® Package Designer</strong></td>
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<td><strong>Allegro FPGA System Planner</strong></td>
<td><strong>Sigtry PowerDC™ and OptimizePI™</strong></td>
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<td><strong>TopXplorer SystemSI for Parallel Bus and Serial Link Analysis</strong></td>
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<td><strong>OrbitIO™ System Planner</strong></td>
<td><strong>Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM</strong></td>
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<td><strong>Advanced Design Verification with the RAVEL Programming Language</strong></td>
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<tr>
<td><strong>Allegro Package Designer Plus</strong></td>
<td><strong>Celsius Thermal Solver</strong></td>
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**Number of days for instructor-led course**: 1, 2, 3

**Tiers of Cadence products used in course**: 1, 2, 3

**Online Course Available**: Yes

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### Custom IC, Analog and RF Design Learning Map

**Circuit Design, Simulation, Modeling and RF Design**

**Analog Modeling with Verilog-A**
- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model
- Behavioral Modeling with Verilog AMS
- Behavioral Modeling with VHDL-AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification
- **Virtuoso Schematic Editor**
- **Virtuoso Visualization and Analysis**
- **Virtuoso ADE Explorer & Assembler Series**
  - S1 ADE Explorer & Single Test Corner Analysis
  - S2 ADE Assembler & Multi Test Corner Analysis
  - S3 Sweeping Variables and Simulating Corners
  - S4 Monte Carlo, Real-Time Tuning & Run Plans
- **Design Checks and Asserts**
- **Virtuoso ADE Verifier Series**
  - S1 Setup, Run, & View Verifier Results
  - S2 Reference Flow and Analog Coverage Using the Setup Library Assistant
- **5G mmWave Handset System Design – S1 RFIC (Transceiver) Design**

**Spectre® Simulator Fundamentals Series**
- **Spectre® Basics**
- **Large-Signal**
- **Small-Signal**
- **Spectre MDL**
- **Spectre Accelerated Parallel Simulator (APS)**
- **Spectre XPS for Mixed-Signal Designs**
- **Virtuoso® Spectre® Pro Series**
  - **DC Algorithm**
  - **AC, XF, STB, Noise**
  - **Transient Algorithm**
  - **Fourier Transform**
  - **Transient Noise**
  - **RF Shooting Newton**
  - **RF Harmonic Balance**

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**Number of days for instructor-led course**: 3

**Tiers of Cadence products used in course**: 1

**Online Course Available**: Yes

**Digital Badge Available**: Yes

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Tensilica Processor IP Learning Map

Tensilica Xtensa NX
- Processor Fundamentals
- Processor Interfaces
- Hardware Verification and EDA
- Instruction Extension Language and Design
- System Modeling using XTSC

ConnX DSP
- ConnX B10 DSP
- ConnX B20 DSP

Vision DSP
- Vision Q7 DSP

New Course
- Number of days for instructor-led course
- Online Course Available

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