Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Mixed Signal Modeling and Verification
- Computational Fluid Dynamics
- Safety and Reliability Platform
- Tensilica® Processor IP
- Reality DC
- Onboarding

cadence®

PCB Design and Analysis Learning Map

Beginner

Advanced

Logic Design

- Allegro X Design Entry HDL Basics — 0.5 day
- Allegro® X Design Entry HDL Front-to-Back Flow — 3 days
- Allegro EDM Design Entry HDL Front-to-Back Flow — 3 days
- Allegro X System Capture Basics — 1 day
- Allegro X System Capture Front-to-Back Flow — 2.5 days
- Allegro Design Reuse — 1 day
- OrCAD® X Capture — 2 days
- OrCAD CIS — 1 day
- OrCAD X Capture Constraint Manager PCB Flow — Accelerated Learning Path Course — 1 day
- Analog Simulation with PSpice® — 3 days
- Analog Simulation with PSpice® using System Capture — 3 days
- Analog Simulation with PSpice® using Design Entry HDL — 4 days

PCB Design

- OrCAD X Presto Basic Techniques — 3 days
- Allegro X PCB Editor Basic Techniques — 3.5 days
  - Allegro X PCB Editor Intermediate Techniques — 2.5 days
  - Allegro X PCB Router Basics — 2 days
  - Allegro X PCB Editor Advanced Methodologies — 1 day
- Allegro X High-Speed Constraint Management — 2 days
- Allegro DesignTrue DFM — Accelerated Learning Path Course — 2 days
- Allegro X Update Training — 2 days
- Advanced Design Verification with the RAVEL Programming Language — Accelerated Learning Path Course — 2 days

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity — 3 days
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials — 2 days
- Sigrity Aurora — 2 days
- Sigrity PowerDC™ and OptimizePI™ — 1 day
- DC and Thermal Analysis with Celsius PowerDC — NEW — 2 days
- PDN and Voltage Ripple Analysis with Sigrity X OptimizePI and SystemPI — NEW — 2 days
- SystemSI for Parallel Bus and Serial Link Analysis — 2 days
- Model Generation and Analysis using PowerSI and Broadband SPICE — 3 days
- Clarity 3D Solver — 2 days
- Celsius Thermal Solver — 1 day

Library Development

- DE-HDL Library Development using DE-HDL — 2 days
- DE-HDL Library Development using Allegro X System Capture — NEW — 2 days
- Allegro X EDM PCB Librarian — NEW — 2 days
- Allegro Design Entry HDL SKILL® Programming Language — 3 days
- Allegro X PCB Editor SKILL Programming Language — 3 days

NEW New Course | # Number of days for instructor-led course | Accelerated Learning Path Course | Online Course Available | Digital Badge Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- Allegro® X Advanced Package Designer
- Allegro Sigrity Package Assessment and Model Extraction
- OrbitIO™ System Planner
- Advanced Design Verification with the RAVEL Programming Language NEW
- Designing with Integrity 3D-IC

SI/PI Analysis

- Sigrity Aurora
- Sigrity PowerDC™ and OptimizePI™
- SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI and Broadband SPICE
- Clarity 3D Solver NEW
- Celsius Thermal Solver

Beginner

Advanced

NEW New Course

Number of days for instructor-led course

Online Course Available

Digital Badge Available

Custom IC/Analog Design and Simulation Learning Map

1 of 3 – see next page

Beginner

Advanced

Circuit Schematic and Design Creation

Virtuoso Schematic Editor

Virtuoso® ADE Explorer & Assembler Series

- **S1** ADE Explorer & Single Test Corner Analysis
- **S2** ADE Assembler & Multi Test Corner Analysis
- **S3** Sweeping Variables and Simulating Corners
- **S4** Monte Carlo, Real-Time Tuning & Run Plans

Analyzing Simulation Results Using Virtuoso Visualization and Analysis NEW

Spectre Simulations

Spectre® Simulator Fundamentals Series

- **S1** Spectre Basics
- **S2** Large-Signal Analyses
- **S3** Small-Signal Analyses
- **S4** Spectre MDL

Design Checks and Asserts In Spectre Simulator

High-Performance Spectre Simulation (APS, Spectre X)

FastSpice Simulations Using Spectre FX Simulator

Spectre FMC in Virtuoso ADE

Virtuoso® Spectre® Pro Series

- **S1** DC Algorithm
- **S2** Transient Algorithm

Virtuoso Spectre Transient Noise

Design Verification

Managing Analog Verification Using ADE Verifier NEW

Reliability Analysis

Reliability Analysis in Virtuoso Studio

Accelerated Learning Path Course

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Custom IC/Analog Physical Design and Verification Learning Map

3 of 3 – see the start

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2
- SKILL Language Programming — 5
- SKILL Development of Parameterized Cells — 2
- Advanced SKILL Language Programming — 3

Photonics

- Virtuoso Layout for Photonics Design - T1 — NEW — 1

Physical Design and Advanced Nodes

- Virtuoso® Layout Design Basics — 1
- Virtuoso Connectivity-Driven Layout Transition — L, XL, GXL, EXL — 2
- Virtuoso Abstract Generator — NEW — EXL — 2
- Virtuoso Floorplanner — GXL — 1

Virtuoso® Advanced Nodes

- Virtuoso Layout for Advanced Nodes — 2
  - T1: Place and Route — 1
  - T2: Electromigration — 0.5
  - Auto Place and Route (APR) for Virtuoso Studio – Device Level — NEW — 2

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — 1
- T2: Create and Edit Commands — 1
- T3: Basic Commands — XL — 1
- T4: Advanced Commands — XL — 1
- T5: Interactive Routing — XL — 1
- T6: Constraint-Driven Flow and Power Routing — XL, GXL — 1
- T7: Module Generator and Floorplanner — Accelerated Learning Path Course — XL, GXL — 1
- T8: Concurrent Layout Editing — EXL — 1
- T9: Virtuoso Design Planner — EXL — 2
- Virtuoso Studio Features — NEW — 2

- Cadence Analog IC Design Flow — NEW — 3

Physical Verification and Extraction

- Pegasus Verification System — NEW — 2
  - Physical Verification System — 2
    - Physical Verification Language Rules-Writer — NEW — 2
- Quantus™ Extraction Solution Transistor-Level Series
  - T1: Overview and Technology Setup — Accelerated Learning Path Course — 0.5
  - T2: Parasitic Extraction — Accelerated Learning Path Course — 1
  - T3: Extracted View Flows and Advanced Features — Accelerated Learning Path Course — 0.5

Accelerated Learning Path Course

NEW New Course | # Number of days for instructor-led course | XL GXL EXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

RF/Microwave and System Design Learning Map

2 of 3 – see next page

Beginner

Advanced

RF Design and Simulations

Virtuoso Schematic Editor — L, XL, 2

Virtuoso® ADE Explorer & Assembler Series

S1 ADE Explorer & Single Test Corner Analysis — 0.5

S2 ADE Assembler & Multi Test Corner Analysis — 1

Spectre® Simulator Fundamentals Series

S1 Spectre Basics — 1

S2 Large-Signal Analyses — 1

S3 Small-Signal Analyses — 1

Spectre® RF Series

RF Analysis Using Shooting Newton — 2

RF Analysis Using Harmonic Balance — 2

System Design

5G mmWave Handset System Design – **S1** Simulation and Verification of the RFIC (Transceiver) — 1

Electromagnetic Analysis

EMX Classic Simulator — NEW — 1

AWR Microwave Design

Microwave & RF Design (AWR®)

Microwave Office for RF Designers — 3

Planar EM Analysis in AWR Microwave Office — 2

3D EM Analysis with Clarity in Microwave Office — NEW — 1

Virtuoso RF Solution

Virtuoso Heterogeneous Integration: EM Analysis of ICs Using the EMX Solver — NEW — 4

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Mixed-Signal Modeling, Simulation and Verification Learning Map

Beginner

Advanced

Circuit Modeling

AMS/Real Number Modeling

- Analog Modeling with Verilog-A — 3 days
- Behavioral Modeling with Verilog AMS — 2 days
- Real Modeling with Verilog-AMS — 2 days
- Real Modeling with SystemVerilog — 3 days

Mixed-Signal Simulations (GUI and Command-Line)

- Virtuoso Schematic Editor — L, XL, 2 days

Virtuoso® ADE Explorer & Assembler Series

- **S1** ADE Explorer & Single Test Corner Analysis — 0.5 days
- **S2** ADE Assembler & Multi Test Corner Analysis — 1 day

Mixed-Signal Design and Simulation

- Mixed-Signal Simulations using Spectre AMS Designer (GUI) — 2 days
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model — 2 days
- SimVision for Debugging Mixed-Signal Simulations — 1 day

Mixed-Signal Verification

- SystemVerilog for Design and Verification — 5 days
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification — 5 days
- Mixed-Signal Verification with UVM — NEW — 1.5 days

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis and Test	Implementation	Silicon Signoff	Equivalence Checking

Semiconductor 101

Digital IC Design Fundamentals

Cadence® RTL-to-GDSII Flow

Fundamentals of IEEE 1801 Low-Power Specification Format

Genus™ Synthesis Solution with Stylus Common UI

Genus Low-Power Synthesis Flow with IEEE 1801

Low-Power Synthesis Flow with Genus Stylus Common UI

Genus Physical Synthesis Flow NEW

Test Synthesis with Genus Stylus Common UI

Advanced Synthesis with Genus Stylus Common UI

ATPG Flow with Modus DFT Software Solution

Joules™ Power Calculator

Design For Test Fundamentals

Innovus™ Block Implementation with Stylus Common UI

Innovus Hierarchical Implementation with Stylus Common UI

Innovus Low-Power Flow with Stylus Common UI

Innovus Clock Concurrent Optimization Technology with Stylus Common UI

Basic Static Timing Analysis

Tempus™ Signoff Timing Analysis and Closure with Stylus Common UI

Voltus™ Power Grid Analysis and Signoff with Stylus Common UI

Conformal® Equivalence Checking

Conformal Low-Power Verification with CPF

Conformal Low-Power Verification Using IEEE1801

Conformal ECO

Cadence® Certus™ Signoff Closure Solution with Stylus Common UI

Virtuoso® Digital Implementation

Artificial Intelligence and Machine Learning Fundamentals

Cadence® Cerebrus™ Intelligent Chip Explorer

NEW New Course | # Number of days for Instructor-led Course | Online Course Available | Digital Badge Available | Accelerated Learning Path Course

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Coverage and Debug

- Digital IC Design Fundamentals — NEW — 2.25
- Xcelium™ Simulator — NEW — 2
- Protium™ Introduction — NEW — 1
- Palladium® Introduction — NEW — 1
- Cadence® RTL-To-GDSII Flow — 2
- Low-Power Simulation with CPF — 2
- Low-Power Simulation with IEEE1801 UPF — 2
- VIP Basic Building Blocks and Usage — NEW — 2
- UCIe VIP Introduction — NEW — 3
- Foundations of Metric-Driven Verification — 1
- Xcelium Integrated Coverage — 2
- Verisium™ Manager — NEW — 3
- vManager Tool Usage in Batch Mode — 0.5
- Verisium™ Debug — NEW — 1
- Perspec™ System Verifier - Basic — NEW — 3
- Xcelium Fault Simulator — NEW — 1.5
- Specman® Fundamentals for Block-Level Environment Developers — 5
- Specman Advanced Verification — 4

NEW New Course | # Number of days for instructor-led course | Accelerated Learning Path Course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application (4)
- VHDL Language and Application (5)
- C++ Language Fundamentals for Design and Verification (3)
- Real Number Modeling with Verilog-AMS (2)
- SystemVerilog for Design and Verification (5)
- SystemC® Language Fundamentals (3)
- Real Number Modeling with SystemVerilog (3)
- SystemC Synthesis with Stratus HLS (3)
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification (5) NEW
- SystemC Transaction-Level Modeling TLM2.0 (2)
- Perl for EDA Engineering (3)
- Tcl Scripting for EDA (2)
- Introduction to TK (1)

UVM

- Essential SystemVerilog for UVM (optional) (1)
- SystemVerilog Accelerated Verification Using UVM (4)
- SystemVerilog Advanced Register Verification Using UVM (2) NEW

- SystemVerilog Assertions (2)
- Jasper® Formal Fundamentals (2)
- Jasper® Formal Expert (2) NEW

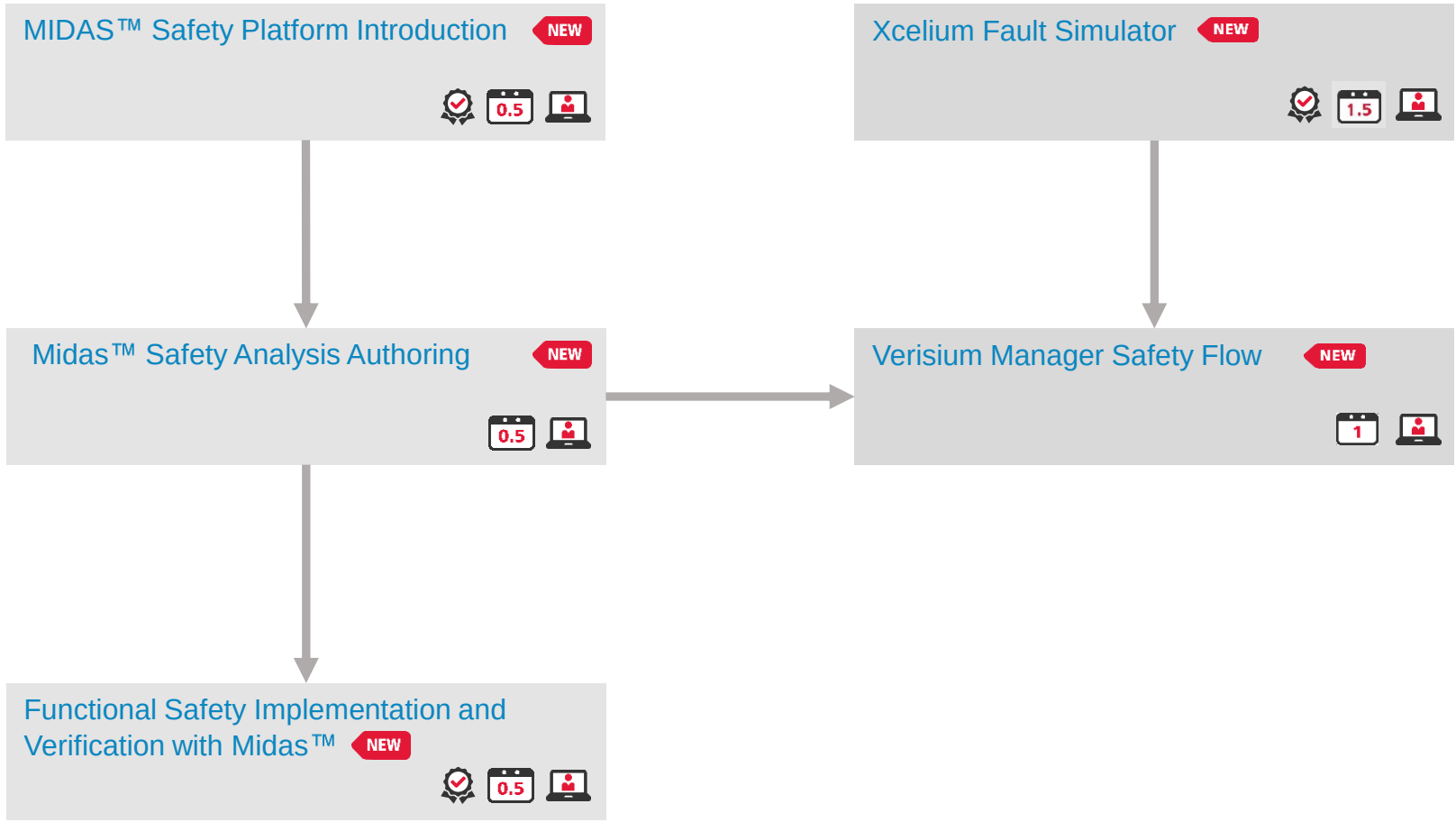
NEW New Course | # Number of days for instructor-led course | Accelerated Learning Path Course | Online Course Available | Digital Badge Available

Safety and Reliability Platform Learning Map

Beginner

Advanced

MIDAS Safety Platform



Beginner

Advanced

NEW New Course

Number of days for instructor-led course

Accelerated Learning Path Course

Online Course Available

Digital Badge Available

Tensilica Processor IP Learning Map

1 of 2 – see next page

Tensilica Xtensa LX

- Tensilica® Xtensa® LX Processor Fundamentals
- Tensilica Xtensa LX Processor Interfaces
- Tensilica Xtensa LX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design
- Tensilica System Modeling using XTSC

ConnX DSP

- Tensilica ConnX DSP Family NEW
- Tensilica ConnX BBE32EP Baseband Engine

Fusion, FloatingPoint & MathX DSP

- Tensilica Fusion F1 DSP
- Tensilica Fusion G3 DSP
- Tensilica FloatingPoint DSP Family
- Tensilica MathX DSP Family NEW

HiFi Audio DSP

- Tensilica Audio Codec API
- Tensilica Xtensa Audio Framework
- Tensilica HiFi 3 Audio Engine ISA
- Tensilica HiFi 4 DSP
- Tensilica HiFi 5 DSP

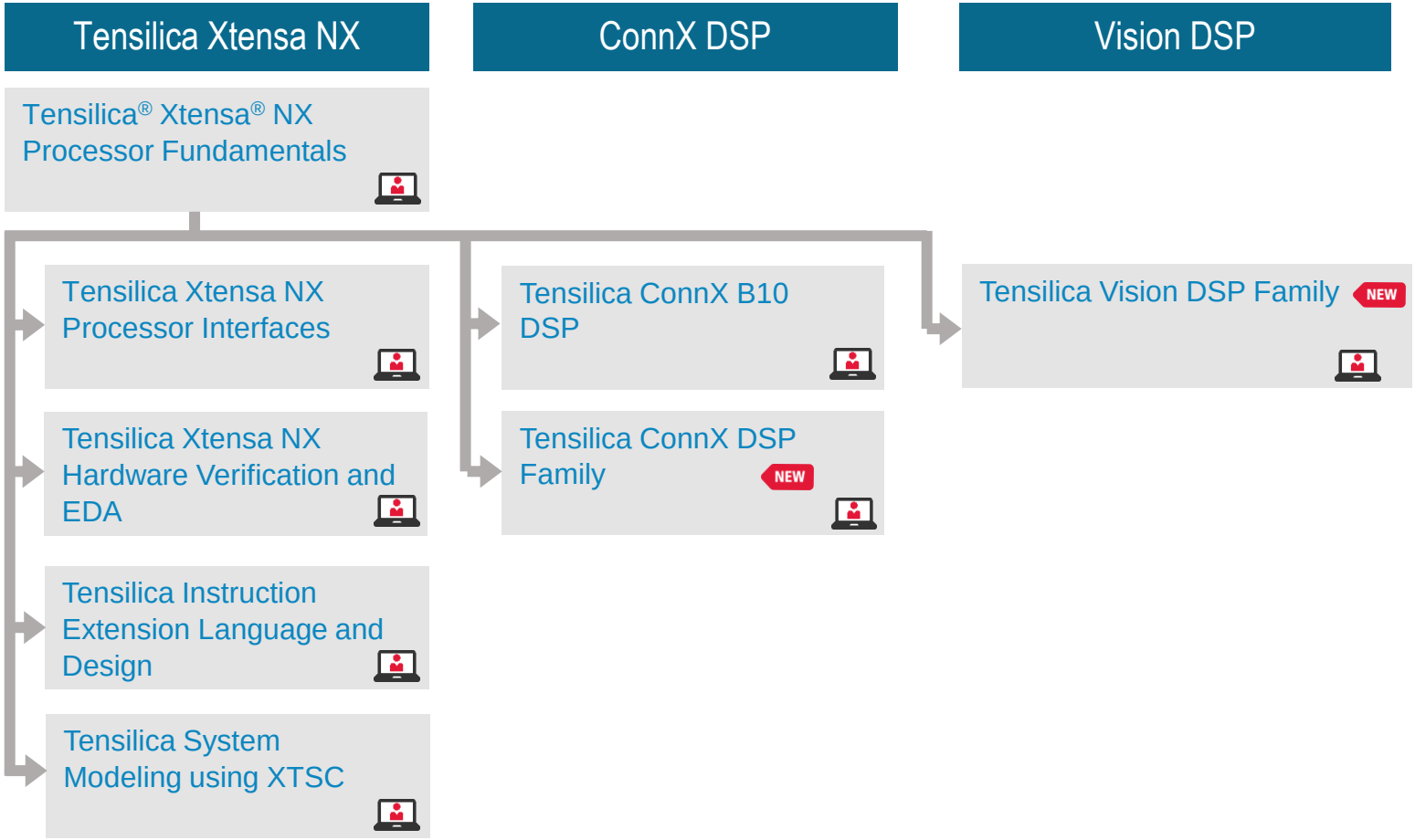
Vision DSP

- Tensilica Vision DSP Family NEW

NEW New Course # Number of days for instructor-led course Online Course Available

Tensilica Processor IP Learning Map

2 of 2 – see prior page



NEW New Course # Number of days for instructor-led course Online Course Available

Computational Fluid Dynamics

Beginner

Advanced

CFD Academy

- CFD Online Course 

Fidelity

Turbomachinery

- Fidelity Turbo: Introduction 

Meshing

- Fidelity Automesh for Unstructured Meshing 
- Fidelity Pointwise Meshing Foundations 

Auto Aero

- Fidelity Flow 

Fine

Marine

- Fine Marine for Beginners 
- Fine Marine for Advanced Users 

NEW New Course

Number of days for instructor-led course

Online Course Available

Digital Badge Available

Reality DC Learning Map

Beginner

Advanced

Design

- Introduction to Data Hall Modeling — 3 days, Online Course Available
- External Environment Modeling — 2 days, Online Course Available
- Transient Cooling Failure — NEW — 0.5 days, Online Course Available
- Flow Network Modeling — 0.5 days, Online Course Available

Insight

Beginner

Advanced

NEW New Course

Number of days for instructor-led course

Online Course Available

Digital Badge Available

Onboarding Curricula

Beginner

Advanced

PCB Design

- PCB Layout Designer Onboarding — 3.75
- Schematic Capture for EEs Onboarding — 6.5
- SI/PI Engineer Onboarding — 6.5
- EE/PCB Layout Designers Onboarding — 6.5

Custom IC, Analog, and RF Design

- Analog Circuit Design and Simulation Onboarding — 6.25
- Virtuoso Layout Onboarding — 5

Mixed-Signal Simulation and Verification

- Analog-Mixed Signal Design Modeling Onboarding — 10

Digital Design and Signoff

System Design and Verification

- System Design and Verification, Digital Physical Design and Signoff Onboarding — 4.4

See also: https://www.cadence.com/en_US/home/training/bridging-the-learning-gap/onboarding-curricula.html

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available