Today, the competition is keener, the challenge is tougher, and that is why Cadence Training is more important than ever!
Cadence Training
Increase Your Value and Effectiveness

Cadence Education Services offers top-notch training and helps you get the most out of your investment. Our classes are developed by experts in the field. They are designed to accelerate productivity and facilitate adoption of Cadence solutions quickly and efficiently.

Technology changes quickly. Keeping your designers up to date on development methodologies and tools through training results in faster development cycles and more capable products – keeping you ahead of the competition.

We invite you to browse through the Cadence Training Brochure and explore the many options Cadence Education Services offers. Find the perfect match for your training needs.

For any further information and requests, please contact your regional Training Coordinator.

Cadence Training Will
- Broaden your knowledge about one specific area or the entire design flow
- Improve the quality of your work
- Increase your productivity
- Keep you current with the newest software features
- Enable you to stay on the productive edge of leading design applications
- Help you better understand how tools work together

The Risks of Doing Nothing
Poorly trained users cost significantly more than well-trained employees because:
- Lower productivity and more rework lead to longer design times and less competitive products
- Negative impact on expert-level workers due to tool-support needs
- Employee frustration causes lower morale and retention
Verilog Language and Application
“Well structured training! Balance between lab exercises and theoretical lessons very well met! Increased my insight on digital development a lot!”
– Erich Loew, NXP Semiconductors

Using Virtuoso Spectre Simulator Effectively
“Electronic lecture and labs are thorough and provide excellent reference material for ongoing training. Instructors were very detail oriented and did a great job explaining the tools and I look forward to more training classes in the future.”
– Donna Azzam, Texas Instruments

SystemVerilog for Design and Verification
“This course was really helpful and I have improved my knowledge with the in-depth introduction and explanation to the subject.”
– Leela Thimmaiah, TU Darmstadt

Specman Fundamentals for Block-Level Environment Developers
“I am completely satisfied with the Specman Basic 5 Day Training. I learned a lot. I can feel an instant improvement. The training material was well organized and topics presented are of great usage. I liked the lab exercises, I liked everything. It is really high quality and the presenter is really good at giving lectures. I feel I enormously improved my knowledge. Thank you for this nice training! Just continue being this good and professional.”
– Marko Ilic, Infineon Technologies

Virtuoso Layout Design Basics
“The course was well organised and allowed me to quickly gain skills with the Virtuoso Layout software. In particular, I learned many useful tricks that allow me to work in a faster and more efficient way.”
– Dr. Giuseppe Moschetti, Fraunhofer Institute

For courses delivered for STMicroelectronics by Cadence Education Services during the year 2013, the “Kirkpatrick” Level 2 evaluation – pre and post quizzes measuring skills acquired during the course – was implemented. The results show 36% of increased skill expertise for Cadence training attendees.
Instructor-Led Training

Benefits of ILT

- Q&A session with live instructor
- Direct interaction with other users
- Focus completely on learning by being away from your usual working environment
- Lecture material detailing tool- and design-related topics
- Hands-on exercises giving you a chance to experiment with the tools and practice the concepts covered during lecture
- Choose from more than 130 classes that are held at our worldwide training centers. Go to our website at www.cadence.com/training, select your region, and browse the course catalog, or contact your training location for dates and details.
- Or request an onsite training for flexible scheduling and a private learning experience, centering on your needs. Another benefit of this option is the elimination of travel-related expenses.

What is ILT?

Instructor-led trainings (ILTs) are live classes that are offered in our state-of-the-art classrooms at our worldwide training centers or at your site. Each is led by an experienced instructor who is an expert in the respective field. The courses are designed and developed to teach a specific tool or design discipline. They contain lecture material, hands-on labs, expert tips and tricks from the instructors, and can even be virtual (see page 6).

ILT Offerings

Standard Training Courses

More than 130 standard training courses are available with predefined sets of topics. They are offered at Cadence training facilities or can be delivered onsite at your facility.

Tailored Training Courses

Tailored training courses offer you the option to mix, add, or eliminate topics from one or more courses. Select your topics of interest, and we will tailor the class for you, using our standard course database.

Custom Training Courses

Custom training courses provide you with maximum flexibility. You can request only certain topics to be covered, new topics to be added, or you can provide your own design or database to use in the labs.

Tailored/custom courses are typically held at a customer site, but can also be offered at Cadence training facilities.
Internet Learning Series
Your Cadence Online Training Solution

Value of Online Training
We understand that it’s not easy to find time in your busy schedule for training. But you know you need training to effectively use the latest software features to sharpen your competitive design edge.

Our Online Training library of courses helps you to get the training you need at times that are convenient for you. Online Training is delivered over the web to let you proceed at your own pace, anytime and anywhere.

The Cadence Online Training solution helps you to stay on the productive edge whenever you want.

Experience Online Training Yourself
1. Login to http://learning.cadence.com in the Cadence Learning Management System (LMS)
2. In the search window, type “preview”
3. Select the online course name and click “launch”

Online Training Offerings
1. Single-User Program: One course, access anywhere, at anytime, on any web browser, for six months unlimited, per student
2. Online Training Subscription: Multiple courses of one or more technology groups, access anywhere, at anytime, on any web browser, for twelve months unlimited, per student

Benefits of Online Training
- Secure online access to dynamic lecture material
- Practice using the lab exercises
- Repeat exercises
- Review information
- Online support for your questions
- Learn at your own pace, anytime and anywhere
- Learn conveniently and cost-effectively without having to travel
- No rigid course schedule
- Fast skill enablement

Additional Benefits of the Online Training Subscription
- Automatic access to any new Online Training course and book that is added to the Online Training collection during the subscription period
- Cost-effective way to access multiple courses
- Increase your knowledge in a technology group
- Increase your value, effectiveness, and flexibility in your design team

Watch Our Video for More Details
Virtual Classroom
Live Training Without the Need to Travel

A Virtual Classroom is a web-based environment that allows you to participate in live training events without traveling. Without additional expenses and travel time, Virtual Classroom makes efficient multi-site training across geographic regions possible.

You listen to lectures, participate in lab exercises, ask questions, and receive feedback just as you would in a conventional classroom, except you do it from the convenience of your desktop or anywhere you have an Internet and phone connection.

Each course is usually divided into four-hour sessions spanning several days. Each session consists of lectures and lab exercises using Cadence software. Between sessions, you can further explore the lab exercises on your own, or you can concentrate on your design projects for the rest of each day.

Categories

No matter which delivery method you prefer, you can choose from a vast selection of trainings categorized as follows:

**Tool**
The focus of tool training is basic usage and how to access technology effectively.

**Engineer Explorer**
The Engineer Explorer (EE) Series is designed for more experienced users of Cadence tools, and provides more sophisticated strategies, tool exploration, and learn-by-doing-techniques. In our learning maps, these are marked with an EE symbol.

**Language and Methodology**
Language and Methodology courses include design and/or language theory and techniques. You will find technical capabilities combined into a consistent and repeatable flow.

**IP**
IP courses quickly get you productive in using Tensilica® baseband, audio, and imaging/video intellectual property (IP). Additional courses cover processor instruction-set extensions and SystemC system modeling.
Methodology-Based Language Training

Multiple-experienced trainers with practical experience in real-world electronic design, state of the science content, worldwide and modern equipped training centers, and more than 4000 satisfied customers per year make us the accepted worldwide leader in methodology-based language training for electronic design.

Find us and our broad variety of courses on www.cadence.com/training and www.esperan.com:

- Language and Methodology Courses for Chip and SPB Design
  - Behavioral Language for AMS Simulation
  - Formal Verification
  - HDL Language
  - HDL Verification
  - High-Speed
  - Script
  - SystemC
  - SystemVerilog

Special offer!
First 100 customers enrolling in our methodology-based language courses:
- Get 1 free* online training of the same technology
- OR
- Take 1 colleague along for free* to live class

*Offer valid worldwide, expires September 30 2014, and is not valid under existing training contract. Use promo code MBLTbrochure 14.

SystemVerilog Advanced Verification Using UVM

“Great overview of UVM. Instructor knew material very well and was very good about answering our sometimes quite out of the box questions.”  
– Jacob Harer, Allegro MicroSystems

SystemVerilog for Design and Verification

“Thanks a lot for last week’s excellent training! I and the other attendees found this training very informative. All we need to do now is to put the learning contents into practice…”  
– Eckart Wagner, Micronas

Specman Fundamentals for Block-Level Environment Developers

“The Cadence Specman training is a great way of learning the e language, the Specman tool, and the Universal Verification Methodology (UVM). The training is a great experience with skilled trainers who have real-world verification experience and cater to the needs of every participant. The well-rounded combination of theory and hands-on exercises make the Cadence training a unique learning experience that helped increase my team's functional verification productivity, and, as such, I highly recommend this Cadence training.”  
– Raimund Soenning, Fujitsu Semiconductor

SystemVerilog Advanced Verification Using UVM

“Excellent course, one of the most effective I’ve attended.”  
– Seamus Ryan, Analog Devices International

Tcl Scripting for EDA + Intro to Tk

“I am pleased about the outcome of this course. The instructor had strong knowledge about Tcl and how to use it in EDA tools.”  
– Evangelos Logaras, NXP Semiconductors

www.cadence.com/training
# Digital Verification, Languages, and Methodologies with Incisive Technology

## Learning Map

### Core
- **VHDL Language and Application**: This course provides a solid background in the use and application of VHDL to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.
- **Verilog Language and Application**: This course provides a solid background in the use and application of Verilog to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.
- **Incisive SystemC, VHDL, and Verilog Simulation**: This course addresses Incisive® mixed-language (SystemC, VHDL, and Verilog) event-driven digital simulation. The course steps you through compilation, elaboration, simulation, and analysis, explaining the most popular options at each step.

### Experienced
- **Incisive Formal Fundamentals with EV and IV (3)**
- **SystemVerilog Assertions (2)**
- **Perl for EDA Engineering (3)**
- **Tcl Scripting for EDA & Introduction to Tk (3)**
- **Verilog Language and Application (4)**
- **VHDL Language and Application (5)**
- **Incisive SystemC, XL VHDL and Verilog Simulation (2)**
- **SystemC Fundamentals (3)**
- **C++ Fundamentals for Design and Verification (2)**
- **SystemC Fundamentals for Block-Level Environment Developers (5)**

### Master
- **Formal Analysis Advanced with Incisive Formal Verifier (2)**
- **SystemVerilog Advanced Verification using UVM (2)**
- **Low Power Simulation with IEEE 1801 UPF (2)**
- **Low Power Simulation with CPF (2)**
- **Incisive Comprehensive Coverage with IMC (2)**
- **Acceleration and Emulation using Palladium XP (3)**
- **Low Power Simulation with CPF (2)**
- **SystemC Synthesis using C-to-Silicon Compiler (3)**
- **Cadence Virtual System Platform (2)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**
- **SystemC Synthesis using C-to-Silicon Compiler (3)**
- **Cadence Virtual System Platform (2)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**

### Palladium
- **SystemVerilog Advanced Register Verification using UVM (2)**
- **Power Aware Emulation with DPA and CPF (2)**
- **SystemC Synthesis using C-to-Silicon Compiler (3)**
- **Cadence Virtual System Platform (2)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**

### SystemC
- **Incisive Formal Fundamentals with IEV and IFV (3)**
- **SystemVerilog for Design and Verification (5)**
- **SystemC Synthesis using C-to-Silicon Compiler (3)**
- **Cadence Virtual System Platform (2)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**

### Specman
- **Specman Advanced Verification (4)**
- **SystemVerilog Advanced Verification using UVM (2)**
- **Power Aware Emulation with DPA and CPF (2)**
- **SystemC Synthesis using C-to-Silicon Compiler (3)**
- **Cadence Virtual System Platform (2)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**

### Also available as a self-paced course. (G) denotes Advance with Engineer Explorer class. L, XL, and GXL denote tiers of Cadence products used in course. Not applicable if no legend. Some course titles may vary. Please refer to your regional catalog for exact titles and course datasheets. (#) denotes number of days for instructor-led training. Several self-paced courses are only available in our Online Training Collection. (NEW) New course (see online course catalog at www.cadence.com for a complete listing of current courses).

## Course Descriptions

### HDL Design Verification with Incisive

#### VHDL Language and Application
This course provides a solid background in the use and application of VHDL to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.

#### Verilog Language and Application
This course provides a solid background in the use and application of Verilog to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.

#### Incisive SystemC, VHDL, and Verilog Simulation
This course addresses Incisive® mixed-language (SystemC, VHDL, and Verilog) event-driven digital simulation. The course steps you through compilation, elaboration, simulation, and analysis, explaining the most popular options at each step.

#### Tcl Scripting for EDA + Intro to Tk
This compact course is the fastest and most effective method for engineers to understand the potential of Tcl for controlling EDA tools and to become proficient in the language. The Tk part teaches how to use widgets to easily create graphical user interfaces (GUI), how to lay out interfaces, and how to “bind” new behaviors to events.
**SystemVerilog for Design and Verification**: This course gives you an in-depth introduction to the main enhancements SystemVerilog adds to Verilog. The course discusses the benefits and issues with the new features and demonstrates how design and verification is more efficient and effective when using SystemVerilog constructs. In particular, the course covers key verification features for randomization, coverage, assertion checking, and object-oriented design.

**Incisive Comprehensive Coverage**: This course explores Incisive comprehensive coverage features, with which you can measure how thoroughly your testbench exercises your design. The course addresses coverage of SystemC, VHDL, Verilog, and mixed-language designs.

**Perl for EDA Engineering**: This course was written from the ground up with EDA professionals in mind. It teaches both basic and advanced concepts of Perl for processing large volumes of data, translating tool output formats, and assisting in general shell and tool tasks. This course is invaluable to anyone working with Perl scripts on a regular basis.

**Verification with PSL**: This course provides a deep introduction to PSL, followed by guidelines and methodologies for describing and debugging complex design assertions for verification, coverage, and formal analysis.

**SystemVerilog Assertions**: This course gives you an in-depth introduction to SystemVerilog Assertions (SVAs), together with guidelines and methodologies to help you create, manage, and debug effective assertions for complex design properties.

**Formal Analysis Fundamentals with Incisive Formal Verifier**: This course introduces the principles of formal analysis and teaches methodology and techniques to enable the most efficient use of Incisive Formal Verifier. The course provides an excellent jump-start for design and verification engineers, with no prior knowledge of formal analysis, to become immediately effective.

**Formal Analysis Advanced with Incisive Formal Verifier**: This advanced course follows on from the Formal Analysis Fundamentals class to address complex issues that can reduce performance. The course examines more advanced formal analysis methodology and tool features, including links to verification planning and management.

**SystemVerilog Advanced Verification Using UVM**: Universal Verification Methodology (UVM) is a class-based verification library and reuse methodology for SystemVerilog. This course describes the verification building blocks and infrastructure provided by UVM, and defines a methodology for creating verification environments with reusable UVM verification components (UVCs). This course also contains an optional review of SystemVerilog class constructs, together with an overview of object-oriented concepts and features.

**SystemVerilog Advanced Register Verification Using UVM**: This course explores the register modeling features of UVM and describes a methodology for controlling, observing, and checking register behavior. You will learn how to create a register model from an XML description, integrate the model into your UVM verification environment, and use standard API calls to create directed and randomized register tests. You will also explore monitoring, prediction, coverage, memory verification and the modeling of special registers.

**Palladium**

**Acceleration and Emulation with Palladium XP**: This course introduces you to using the Palladium® XP verification computing platform for accelerating the verification of design. The course steps you through preparing a design for emulation, running a simulation, debugging the results, improving simulation performance, dynamic power analysis (DPA) and power-shutoff system verification using the Common Power Format (CPF).

**SystemC**

**C++ Language Fundamentals for Design and Verification**: This course provides an introduction to the C++ programming language for design and verification engineers, covering classes, variables and functions, constructors, destructors, inheritance and polymorphism.

**SystemC Language Fundamentals**: This course teaches the IEEE standard 1666-2005 SystemC language and explores how it can be used for system, hardware, and verification modeling.

**SystemC Transaction-Level Modeling (TLM 2.0)**: This course teaches the IEEE SystemC TLM 2.0 library, showing you how to develop loosely-timed and approximately-timed models and how to use the debug capabilities of TLM2.0.

**SystemC Synthesis using C-to-Silicon Compiler**: This course introduces hardware designers to high-level synthesis. It introduces the SystemC language, examines the SystemC coding style for high-level synthesis, and explores micro-architectural alternatives in the context of the Cadence C-to-Silicon Compiler.

**Specman**

**Specman Fundamentals for Block-Level Environment Developers**: This course is an introduction to the e language and the Incisive Enterprise Specman Elite Simulator. The course is based on a coverage-driven verification methodology, which is applicable for a broad range of designs. The course shows how to create a reusable, block-level verification environment and then how to instantiate, customize, and write tests for this environment. The verification methodology taught by this class is compatible with the Universal Verification Methodology (UVM).

**Specman Elite Advanced Verification**: This advanced course follows on from the Specman Fundamentals class to provide a much greater understanding of the e language and the Specman tool. This course covers advanced language and tool techniques and examines how to scale verification environments from a block to system level while obtaining maximum reuse of your Verification IP.

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**SystemVerilog Advanced Verification Using UVM**

“I have a dream: I can reuse my favourite testbench in every new product and…
This dream came true after the Cadence UVM class!”

– Joerg Keber, NXP Semiconductors
## PCB and Package Design with Allegro Technology

### Learning Map

<table>
<thead>
<tr>
<th>Logic Design</th>
<th>PCB Design</th>
<th>Signal Integrity</th>
<th>IC Package Design</th>
<th>Library Development</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analog Focus</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allegro AMS Simulator Adv. Analysis (1)</td>
<td>Allegro RF PCB (1)</td>
<td>Allegro Sigrity System-Level Serial Link Analysis (1)</td>
<td>Allegro PCB Editor ESKILL Language (3)</td>
<td></td>
</tr>
<tr>
<td>Allegro AMS Simulator (3)</td>
<td>Analog Simulation with Pspice (3)</td>
<td>Allegro Sigrity PI (1)</td>
<td>Allegro Design Entry HDL SKILL Language (3)</td>
<td></td>
</tr>
</tbody>
</table>

| Master | | | | |
| Allegro FPGA System Planner (2) | OrCAD TCL (2) | Allegro GRE Interconnect Flow Planning (2) | Allegro Sigrity Power-Aware Parallel Bus Analysis (2) | Allegro Design Workbench for Administrators (2) |
| Allegro Design Workbench for Engineers and Designers (1) | Allegro Team Design Authoring (1) | Allegro PCB Editor Intermediate Techniques (2) | Allegro Sigrity Power Integrity Suite (1) | |
| | | Allegro Design Entry Using Orcad Capture (2) | | |
| | | Allegro Design Entry HDL Front-to-Back Flow (3) | | |

| Experienced | | | | |
| Allegro Design Reuse (1) | Allegro Design Workbench for Engineers and Designers (1) | Allegro PCB Editor Intermediate Techniques (2) | Allegro Design Workbench for Administrators (2) |
| Allegro System Architect (1) | Allegro Team Design Authoring (1) | Allegro Sigrity Package Assessment and Model Extraction (1) | |
| | | Allegro High-Speed Constraint Management (2) | |
| | | Allegro Tool Setup and Configuration (2) | |

| Core | | | | |
| Allegro Design Entry HDL Basic Techniques (3) | Allegro Design Entry Using Orcad Capture (2) | Allegro Sigrity SI Foundations (2) | Allegro Package Designer (4) |
| Allegro Design Entry Using Orcad Capture (2) | Allegro PCB Router Basics (2) | Understanding High Frequency PCB Design: High-Speed, RF, and EMI (5) | Allegro PCB Librarian (2) |
| | | | | |
| | | | | |

Also available as a self-paced course. (EE) denotes Advance with Engineer Explorer class. (L, XL, and GXL) denote tiers of Cadence products used in course. Not applicable if no legend. Some course titles may vary. Please refer to your regional catalog for exact titles and course datasheets. (#) denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](www.cadence.com). New course (see online course catalog at www.cadence.com for a complete listing of current courses).

### Course Descriptions

#### Allegro High-Speed Constraint Management
This course covers the application and verification of high-speed constraints across a design process. You learn to schedule nets, control impedance on nets, control the propagation delay from drivers to receivers, and match the propagation delay of driver and receiver pairs.

#### Allegro Tool Setup and Configuration
This course teaches you how to create a customized setup for many Allegro® tools that can be applied to a single user or across an entire company site. This tool setup course makes it easier for you to use the Allegro tools, to get new designs started, and to establish a standard environment that maximizes productivity.

#### Logic Design

**Allegro Design Entry HDL Front-to-Back Flow**: This course teaches you how to create board-level schematic designs and demonstrates the integration between Design Entry HDL and other tools in the design flow, including the PCB Editor.

**Allegro Design Entry Using OrcAD Capture/OrcAD Capture CIS**: This course covers front-end design processes such as setting up design templates, creating a netlist for board layout, and part management. The OrcAD® Capture CIS class covers the CIS database, adding parts to the schematic, and modifying part properties.
Allegro System Architect: The course introduces you to a new paradigm in design entry, making use of a spreadsheet- or table-based System Connectivity Manager tool.

Allegro Team Design Authoring: In this course, you’ll learn how a three-person team can use the Team Design software to concurrently create and integrate different parts of a hierarchical design. The Team Design software is also used to manage the concurrent layout of multiple physical partitions on the PCB.

Allegro Design Reuse: Design reuse is the creation of a logical block and physical layout representing a standalone portion of a design. The logical and physical data is placed in a library for others to reuse.

Allegro Design Workbench for Engineers and Designers: This course shows you how to create a new project, search and add parts to your schematic using the component browser, take the design to layout, and back annotate.

Allegro FPGA System Planner: This course shows you how to define your FPGA system and synthesize the connections in your design. You generate a schematic and PCB Editor database so the FPGA I/O assignments can be optimized in the board environment.

OrCAD TCL: This class will instruct the student how to use a scripting functionality to execute an OrCAD Capture command through a command prompt. Note: This class is in development and is expected to be released the second half of 2014.

Allegro AMS Simulator: This three-day course starts with the basics of entering a design for simulation and builds a solid foundation in the overall use of the various simulations available in the Allegro AMS Simulator product.

Analog Simulation with PSpice: This three-day course starts with the basics of entering a design for simulation and builds a solid foundation in the overall use of the various simulations available in the Allegro AMS Simulator product.

Allegro AMS Simulator Advanced Analysis: In this course, you configure and run advanced analyses, including sensitivity, Monte Carlo, stress, and worst case. This course uses the Design Entry HDL schematic entry tool.

PSpice Advanced Analysis: In this course, you configure and run advanced analyses, including Monte Carlo, stress, sensitivity, and worst case. This course uses the OrCAD Capture schematic entry tool.

PCB Design

Allegro PCB Router Basics: This course teaches you how to use the Allegro PCB Router and interactive wire editing tools.

Allegro PCB Editor Basic Techniques: This course covers all the necessary steps for designing a PCB, from loading logic and netlist data, through producing manufacturing/NC output. This course is a prerequisite to the Allegro PCB Editor Intermediate Techniques course.

Understanding High Frequency PCB Design

“...The course helped to structure the theoretical knowledge I already had, brought some new technical aspects but most of all I liked the practical aspects...

– Claudia Goga, Digilent
Allegro PCB Editor Intermediate Techniques: This course gives you a deeper understanding of the software and presents features and tips. In the task-oriented labs, you use a combination of interactive and automatic tools. You should attend the Allegro PCB Editor Basic Techniques course before attending this course, or have the equivalent work experience.

Allegro PCB Editor Miniaturization: In this course, you explore the utilities and programs in the Allegro PCB Editor Miniaturization option. You use blind/buried vias in a design, High Density Interconnect (HDI) design, fanouts for BGA devices using HDI, embedded components, and manual routing in flex designs. You must have a license for the Miniaturization option to get the most from this course.

Allegro GRE Interconnect Flowplanning: The Global Route Environment (GRE) provides the technology and methodology to capture as well as adhere to a designer's intent. In this course, you apply this technology and methodology to convert your design intent into the final board design.

Allegro RF PCB: In this course, you learn about various RF PCB front-to-back flows.

Signal Integrity

Understanding High-Frequency PCB Design—High Speed, RF, and EMI: Part 1 of this two-part course applies basic physical principles to develop an understanding of the issues of high-speed design, thereby ensuring a successful design for signal integrity. Part 2 builds on the principles and practices established in Part 1, extending them to develop techniques for design and test at frequencies above 1GHz for Gbps serial transmission and for controlling the generation and propagation of EMI at the PCB level.

Allegro Sigrity SI Foundations: In this course, you use the Allegro Sigrity™ SI software to develop design rules for high-speed designs. You add the resulting physical and electrical constraints to the design through topology templates. These constraints drive the routing of nets on the PCB. You run preroute and postroute signal simulations to analyze the PCB for reflection, crosstalk, and other high-speed design factors.

Sigrity Power Integrity Suite: This class covers the Sigrity Power Integrity Suite which includes PowerDC to perform Static IR Drop Analysis, PowerSI to extract SI models, and OptimizePI to perform AC Power Plane analysis to optimize capacitor selection and placement.

Allegro PCB Editor Basic Techniques

“I already knew the basics but I learned a lot of stuff to speed my work up and make it easier.”
– Johannes Woehr, Schunk
Allegro Sigrity Power-Aware Parallel Bus Analysis:
This class covers the analysis of a DDR2 parallel bus interface to verify the operation of the bus using System SI Parallel Bus Analysis.

Allegro Sigrity PI: This class covers the Allegro Sigrity PI product which provides an integrated solution for power delivery analysis and features integrated Sigrity technology for DC analysis and a Power Feasibility Editor to drive the creation of Power Integrity Constraint Sets.

Allegro Sigrity System-Level Serial Link Analysis: In this class, you will simulate and use modeling techniques available for the design and analysis of serial data channels.

SiP Sigrity SI Foundations: In this course, you analyze the high-speed nets in a multi-chip module. You use the Topology Editor to extract topologies from the design for analysis and create your own topologies to explore design technology tradeoffs.

IC Package Design

SiP Layout: This course takes you through a complete design flow of a system-in-package (SiP) design, from defining the module outline, through placing components, defining a netlist, placement, routing, documentation, and manufacturing output. The course covers the complete design flow for a flip-chip and wire-bonded stacked die module using the Cadence SiP Digital Layout software.

Allegro Package Designer: This course discusses the Allegro Package Designer system. It covers the design and specifications for manufacturing single-chip modules for single-, double-, or multi-layered analog and digital packages.

Allegro Sigrity Package Assessment and Model Extraction: This class covers the extraction of both a SPICE model and an IBIS model for a package as well as the assessment of the power and ground distribution system and the signal distribution of the package. You start by translating a package design into the XtractIM environment and then identify the coupled lines in the package. You extract two types of SPICE models and two types of IBIS models for the package. You use the package assessment features in XtractIM to plot the broadband impedance of the package distribution system and then examine the RLC distributions for each pin of the package. Finally, you plot the insertion loss and the return loss for the nets in the package design.

SiP RF Architect: In this course, you use a design flow between the Virtuoso® design environment and the SiP Layout environment. You use this flow to create a single, system-level, circuit simulation-ready schematic for an RF/analog die, SiP substrate, and for packaged and embedded discrete devices.

Library Development

Allegro Design Workbench for Librarians: In this course, you will learn how to create a new project, new parts, new schematic models, and new footprint models. You will also be taken through an ECO flow to update an existing part.

Allegro PCB Librarian: In this course, you are introduced to the Library Explorer, the Part Developer, and PCB Editor. Next, you learn how to create a development and testing area for new Allegro Design Entry HDL (DE-HDL) and PCB Editor parts.

Allegro Design Workbench for Administrators: This course is designed for users responsible for updating and maintaining the Allegro Design Workbench environment and databases.

Allegro Design Entry HDL SKILL Language: This course provides the basic knowledge required to begin writing useful commands and functions to customize and extend the functionality of the base Design Entry HDL tool set.

Allegro PCB Editor SKILL Language: This course provides the basic knowledge required to begin writing commands and functions to customize and extend the functionality of the base PCB Editor and Advanced Package Designer (APD) tool set.

“Everything was to my satisfaction and the trainer was excellent.”
– Marcus Olpp, Valeo
### Custom Design with Virtuoso Technology

#### Learning Map

<table>
<thead>
<tr>
<th>IC CAD</th>
<th>Analog, Mixed-Signal and RF Design</th>
<th>Physical Design</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Master</strong></td>
<td><strong>Experienced</strong></td>
<td><strong>Core</strong></td>
</tr>
<tr>
<td>Advanced SKILL Language Programming (3)</td>
<td>Virtuoso AMS Designer (2)</td>
<td>Analog-on-Top (AoT) Mixed-Signal Implementation (2) – uses IC and EDI</td>
</tr>
<tr>
<td>SKILL Programming for IC Layout Design (2)</td>
<td>For Analog (1) For Digital (1)</td>
<td>Using Virtuoso Constraints Effectively (2)</td>
</tr>
<tr>
<td>SKILL Development of PCells (1)</td>
<td>Virtuoso Electrically-Aware Design w/ Layout Dependent Effects (2)</td>
<td>Virtuoso Connectivity-Driven Layout (2)</td>
</tr>
<tr>
<td>SKILL Language Programming (5)</td>
<td>New</td>
<td>New</td>
</tr>
<tr>
<td>SKILL Language Programming Introduction (2)</td>
<td>New</td>
<td>New</td>
</tr>
<tr>
<td>Virtuoso Analog Design Environment (3)</td>
<td>New</td>
<td>New</td>
</tr>
<tr>
<td>Virtuoso Schematic Editor (2)</td>
<td>New</td>
<td>New</td>
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<tr>
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<td>New</td>
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### Course Descriptions

#### Advanced Nodes

**Virtuoso Layout for Advanced Nodes:** Virtuoso ICADV physical design flow, including a review of the advanced node (20nm and below) process and technology requirements, double patterning (DPT), layout dependent effects (LDEs), creating interconnect, streaming in/out pre-colored data, device placement constraints, diffusion rules, end cap poly shares, and poly matching.

**Virtuoso Simulation for Advanced Nodes:** Virtuoso ICADV front-end re-simulation flow with Virtuoso ADE-XL including LDEs that affect your design at advanced nodes of 20nm and below. You’ll use a new simulation flow considering these LDEs with schematic parasitics early in the design flow. Rapid Analog Prototyping, which uses the Constraint Manager and the Circuit Prospector, plays a big part in the flow. In addition, you’ll apply two re-simulation methods, one that uses MODGEN constraints, and one that uses a partial layout in which there is no routing as yet.

#### IC CAD

**Virtuoso Design Environment Setup:** Learn to install the software, manage licenses, and troubleshoot file-locking issues.

**Virtuoso Design Environment:** This course covers administration, such as installing the software, managing licenses, using PDKs, customizing the environment, troubleshooting file-locking issues, and using SKILL commands.

**SKILL Language Programming Introduction:** Get the basic SKILL language foundation to write and debug SKILL procedures in just two days.

**SKILL Language Programming:** This course provides the comprehensive foundation, concepts, and sample programs to build SKILL programs.
SKILL Development of Parameterized Cells: Use SKILL to develop Pcells, the building blocks needed to leverage the connectivity-driven design environment for productivity gains.

SKILL Programming for IC Layout Design: Learn how to use SKILL programs to automate layout tasks.

Advanced SKILL Language Programming: This course focuses on the lexical scoping and object-oriented extensions to the SKILL language, known as SKILL++. You will also use macros to improve your programs.

Digital Implementation Basics for Analog/Mixed-Signal Designs: Learn to use Encounter® Digital Implementation System to implement your AMS designs. Explore floorplanning, placement, power planning, clock-tree synthesis, timing optimization, and detail routing. This course is typically offered as the optional first day of the AoT Mixed-Signal Implementation course for new Encounter users.

Analog, Mixed-Signal and RF Design

Virtuoso Schematic Editor: Learn how to create schematics, their corresponding symbols, and navigate a design hierarchy. Create design constraints using the Constraint Manager and the Circuit Prospector, and learn to use inherited connections.

Virtuoso Analog Design Environment: Learn how to simulate analog circuits in the ADE-L environment using Spectre® and APS Simulators. Use the ViVA XL Waveform Viewer and analyze simulation results. Modify the CDF for an instance. Perform device checking and run parametric sweeps. Use the Hierarchy Editor to switch between multiple design views. Use Virtuoso Power System to evaluate IR drop and electromigration.

Virtuoso Analog Simulation Techniques: Using the ADE-XL environment, learn to simulate multiple testbenches simultaneously using various assistants and workspaces. Perform multiple sweeps and corners analyses, parameterize your design, simulate to meet specs, perform Monte Carlo analysis, and create datasheets.


Virtuoso Electrically-Aware Design with Layout Dependent Effects: Implement a parasitic-aware incremental simulation flow. Perform parasitic estimation and re-simulation using RC values extracted from electrical effects, which occur due to electromigration. Consider electromigration and layout-dependent effects earlier in the design cycle. This becomes critical at advanced nodes.

Virtuoso AMS Designer: Learn to run and debug large, complex mixed-signal/mixed-language simulations using Verilog, Verilog-A, Verilog-AMS, schematic views, Spectre, and SPICE design blocks in mixed configurations. Learn about the concept of discipline resolution and insertion of connect modules. Run AMS Designer using irun from the command line and from the ADE GUI. Debug simulations using SimVision. Use the AMS Incisive flow for design verification. Create real-valued models using the wreal capability.

SKILL Language Programming

“Very good training, will improve my output and inspire my future work. Very experienced instructor, no improvements.”

– Christian Stern, Lantiq
Virtuoso AMS for Digital Designers: Use the mixed-signal, mixed-language Virtuoso AMS Simulator. Use the command-line control-based model and the irun executable. Learn about the concept of discipline resolution and insertion of connect modules. Use the Hierarchy Editor to create design configurations, the SimVision tool to debug simulations and behavioral modeling with the Verilog-AMS mixed-signal modeling language. Learn the Incisive mixed-signal verification flow and Verilog testbench reuse with information on the SystemVerilog language, the System C language, the Common Power Format (CPF), the MATLAB language, and the Simulink coder.

Virtuoso AMS for Analog Designers: Use the mixed-signal, mixed-language Virtuoso AMS Simulator. You use the ADE graphical-interface model and the irun executable. You’ll learn about the concept of discipline resolution and insertion of connect modules. You’ll use the Hierarchy Editor to create design configurations. In addition to the Virtuoso Visualization and Analysis XL waveform viewer, you’ll use the SimVision tool to debug simulations. You’ll use the AMS simulator with the UltraSim solver.

Behavioral Modeling with Verilog-AMS or VHDL-AMS: These courses provide an in-depth approach to writing realistic behavioral models of analog/mixed-signal design blocks and systems using either Verilog or VHDL languages.

Real Modeling with Verilog-AMS: In this advanced Engineer Explorer course, you learn how real number modeling using Verilog-AMS (wrealr) enables high performance digital-centric mixed-signal verification. You must have a working knowledge of the Virtuoso AMS Designer simulator or meet the course prerequisite by taking the Virtuoso AMS Designer course.

Virtuoso Spectre Circuit Simulator: Use Spectre Simulator from the command line to run complex simulations. Learn about Spectre-SPICE compatibility. Examine and run DC, transient, reliability, Monte Carlo, and small-signal analyses from the command line. Learn how to use the APS Option and Spectre MDL.

Spectre Simulations Using Virtuoso ADE: Set up and run Spectre analyses using the Virtuoso Analog Design Environment. Use available Spectre parameters to set convergence and accuracy criteria. Run Spectre simulations, save the results in different database formats, and plot waveforms in the Virtuoso Visualization and Analysis (ViVA) XL tool. The analyses include transfer function, S-parameter, noise, stability, pole-zero, Fourier, and mismatch.

High-Performance Simulation with Spectre (APS/XPS): Use the enhanced technologies of Virtuoso Spectre Circuit Simulator, including the Accelerated Parallel Simulator (APS) and the eXtensive Partitioning Simulator (XPS), to run fast and accurate analog simulations on large, complex, mixed-signal designs providing a significant performance gain over baseline Spectre simulation.

Virtuoso UltraSim Full-Chip Simulator: Learn how to use this FastSPICE simulator to run large transistor-based simulations, including an extensive set of checking commands, power analyses, and IR drop and electromigration tests.

Simulation and Analysis with OCEAN: Explore how to use OCEAN to run analog/mixed-signal simulations and to manipulate your simulation results.

Analog Modeling with Verilog-A: Use Virtuoso ADE and Spectre Simulator to simulate analog circuits using Verilog-A models. Use Verilog-A to model and design an analog-to-digital converter and parts of a PLL.

Using Virtuoso Spectre Simulator Effectively: Get an in-depth look at Spectre Simulator. Learn about DC and AC analysis algorithms and how they affect simulation. Learn how transient analysis simulates and how to evaluate DFT.

RF Analysis with Virtuoso Spectre Circuit Simulator: Learn about the Spectre RF Simulation Option. Set up, simulate, and analyze various RF designs in a receiver chain. Run PSS and QPSS analyses using the Shooting Newton and Harmonic Balance algorithms. Perform noise analysis, evaluate jitter, and learn about envelope analysis.

Physical Design

Virtuoso Layout Design Basics: Learn the basic techniques for working with Virtuoso Layout Suite L. Create and edit cell-level designs utilizing design assistants, and place instances to build hierarchy for custom physical designs.

Virtuoso Connectivity-Driven Layout Transition: This course guides the Virtuoso Layout Suite L user into the Virtuoso Layout Suite XL and GXL tiers. Understand the differences between the tiers and what drives the connectivity between the schematic and layout in XL/GXL.

Virtuoso Layout Pro Series: Half-day courses focused on improving your productivity.

Virtuoso Layout Pro T1—Environment and Basic Commands (VLS-L): Use the latest Virtuoso Layout Suite L features. Customize your working environment to improve your experience when creating layout. Also take advantage from the new user interface features to perform editing operations while minimizing the need of zooming in.

Virtuoso Layout Pro T2—Create and Edit Commands (VLS-L): Use the advanced features introduced in Virtuoso Layout Suite L. Use commands to automate the creation of layout shapes that will improve the way you manage the objects in your design. Examine the differences between paths and wires and how to take advantage of the wires in everyday layout tasks.

Virtuoso Layout Pro T3—Basic Commands (VLS-XL): Work with Virtuoso Layout Suite XL to create layout using a connectivity-driven flow. Start with the creation and placement of layout building blocks, using manual and automated methods. Gain knowledge of the new extractor/binder and learn how to debug problems in the design connectivity. Learn how Constraint Groups affect your layout work.
Virtuoso Connectivity-Driven Layout

“Good tool with nice features which help the designer to improve efficiency.”
– Noureddine Senouci, ON Semiconductor

Virtuoso Schematic Editor

“Efficient course for me to get started with the Virtuoso environment. I appreciated the small group and that I had enough time to do the labs.”
– Stefan Ganserer, Intel

Virtuoso Layout Pro

“Within our internal training analysis, the customized Virtuoso Layout Pro training has reached the best score since 2003.”
– Andre Vullhorst, NXP Semiconductors

Virtuoso Space-Based Router

“Very good course. I learned a lot and I am impressed by the presented features. I am sure that most things I learned the last two days will help me to improve my efficiency. The presenter did a perfect job. Thanks Cadence!”
– Eric Schaefer, IMMS GmbH

Virtuoso Layout Pro T4—Advanced Commands (VLS-XL):
Use the clone and copy commands in Virtuoso Layout Suite XL to reuse already completed portions of your layout design in a connectivity-driven layout flow. You will become familiar with the process of updating your layout after an ECO. Take advantage of design-rules-driven editing to improve your productivity.

Virtuoso Layout Pro T5—Interactive Routing (VLS-XL):
Increase your productivity using the assisted features included in the “Create Wire” family of commands included in Virtuoso Layout Suite XL. Examine the different degrees of automation available to route wires taking advantage of the existing connectivity information.

Virtuoso Connectivity-Driven Layout: Use example IC layouts to explore schematic-driven layout techniques. Virtuoso Layout Suite XL provides many features and automation improvements to assist you.

Using Virtuoso Constraints Effectively: Set specific rules in the schematic that will be transferred to the layout. The specific rules are called constraints, which are more than foundry design rules. The circuit prospector searches for commonly understood configurations of devices or nets. When they are found, the designer can assign constraints that are passed to the layout, such as common centroid, matched parameters, symmetrical placement, or routing constraints.

Virtuoso Floorplanner: Use the floorplanner to calculate the area needed for the top-level boundary and blocks. Place the I/O pads, generate and place the top-level blocks, and complete a top-level floorplan.

Virtuoso Space-Based Router: Space-Based Router runs within Virtuoso Layout Suite GXL. Learn how to quickly capture and manage block- and chip-level routing solutions using the Process Rules Editor as well as customized Tcl scripts.

Virtuoso Layout Suites Update Training: Get detailed explanations of the new features in the IC 6.1.6 release for VLS L, XL, and GXL. View embedded demos that highlight and describe many of the new and improved features. There are extensive notes for clarity and ease of understanding.

Virtuoso Physical Design Update: Learn about the new layout design features, GUI, and use models of the 6.1 platform. This course is designed for those familiar with previous releases (such as 5.1.4.1) who are moving to the new platform; it does not cover migration steps.

Analog-on-Top Mixed-Signal Implementation: This two-day course focuses on the interoperability between digital (Encounter) and analog (Virtuoso) environments, which share a common database. Set up the environment and drive the flow to create and insert a digital block into an analog custom IC design. The first day is the optional Digital Implementation Basics for AMS Designs course.
## Silicon Sign-Off and Verification

### Learning Map

<table>
<thead>
<tr>
<th>Parasitic Extraction</th>
<th>Timing Analysis</th>
<th>Physical Verification</th>
<th>Power Analysis</th>
<th>Design for Manufacturing</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Master</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cadence QRC Techgen Developer (2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cadence QRC RF Transistor and Substrate-Level Extraction (2)</td>
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<tr>
<td><strong>Experienced</strong></td>
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<tr>
<td>Basic Static Timing Analysis (2)</td>
<td>Assura Rules-Writer (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Core</strong></td>
<td></td>
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</tbody>
</table>

▲ Also available as a self-paced course. ▲ denotes Advance with Engineer Explorer class. L, XL, and GXL denote tiers of Cadence products used in course. Not applicable if no legend. Some course titles may vary. Please refer to your regional catalog for exact titles and course datasheets. (#) denotes number of days for instructor-led training. Several self-paced courses are only available in our Online Training Collection. New course (see online course catalog at www.cadence.com for a complete listing of current courses).

### Course Descriptions

#### Parasitic Extraction

**Cadence QRC Techgen Developer**: Get an overview of parasitic extraction, and then use existing RCX or QX tech files to create a tech file for the new QRC extractor.

**Cadence QRC User Transistor-Level Extraction**: This course covers Cadence QRC transistor-level parasitic extraction for analog and full-custom circuits.

#### Timing Analysis

**Basic Static Timing Analysis**: In this course, you learn the basic concepts of static timing analysis and apply them to constrain a design.

**Tempus Signoff Timing Analysis and Closure**: This course is a detailed exploration of the timing, IR drop, and signal integrity analysis capabilities of the Tempus™ Timing Signoff Solution software.
Physical Verification

**Cadence Physical Verification System**: Learn practical methods of running and debugging DRC, ERC, and LVS. Use the powerful PVS debugging environment to locate errors and fix real problems quickly.

**Cadence Assura Verification**: Learn about all aspects of using Assura® tools for design rule checks, short location, and layout versus schematic checks.

**Assura Rules Writer**: Learn how to write and optimize rules for Assura physical verification.

**Physical Verification Language Rules-Writer**: You learn the basic rules and syntax used for writing physical verification language (PVL) rules. The basics include inputs, outputs, runset structures, and differences from Assura rule writing, introduction to new commands, and examples of new command usage.

Power Analysis

**Voltus Power-Grid Analysis and Signoff**: In this course, you explore the need for power-rail analysis and use the Voltus™ IC Power Integrity Solution software power consumption and power rail verification software to run several types of power-consumption and power-rail analyses.

Design for Manufacturing

**MaskCompose Automated Reticle Design Synthesis**: Learn how to define a flow and process, build a reticle layout, produce documentation, generate a wafer layout, and use techniques that accelerate the DFM process.
# Digital Design with Encounter Technology

## Learning Map

<table>
<thead>
<tr>
<th>Logic Design</th>
<th>Place-and-Route</th>
<th>Signoff and Analysis</th>
<th>Design Verification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Master</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advanced Synthesis with Encounter RTL Compiler (1)</td>
<td>Analog-on-Top Mixed-Signal Implementation (2)</td>
<td>Voltus Power-Grid Analysis and Signoff (2)</td>
<td>Encounter Conformal ECO (1)</td>
</tr>
<tr>
<td><strong>Experienced</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Encounter Test Jump Start to ATPG (1)</td>
<td>Low-Power Synthesis Flow with Encounter RTL Compiler (1)</td>
<td>Low-Power Flow with Encounter Digital Implementation (1)</td>
<td>Low-Power Verification with Encounter Conformal (1)</td>
</tr>
<tr>
<td>Test Synthesis Using Encounter RTL Compiler (1)</td>
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<td>Low-Power Synthesis Flow with Encounter RTL Compiler (1)</td>
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<tr>
<td><strong>Core</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Encounter RTL Compiler (2)</td>
<td>Encounter Digital Implementation (Hierarchical) (1)</td>
<td>Tempus Signoff Timing Analysis and Closure (2)</td>
<td>Logic Equivalence Checking with Encounter Conformal EC (2)</td>
</tr>
<tr>
<td></td>
<td>Encounter Digital Implementation (Flat) (3)</td>
<td>Basic Static Timing Analysis (2)</td>
<td>Encounter Conformal Constraint Designer (1)</td>
</tr>
<tr>
<td></td>
<td>Prototyping and Partitioning with First Encounter (2)</td>
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<td>Digital Implementation Basics for Analog Mixed-Signal Designs (1)</td>
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</tbody>
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⚠️ Also available as a self-paced course. 🗻 denotes Advance with Engineer Explorer class. XL, ✔️, and GXL denote tiers of Cadence products used in course. Not applicable if no legend. Some course titles may vary. Please refer to your regional catalog for exact titles and course datasheets. (#) denotes number of days for instructor-led training. Several self-paced courses are only available in our Online Training Collection. 🌐 New course (see online course catalog at www.cadence.com for a complete listing of current courses).

## Course Descriptions

### Logic Design

**Encounter RTL Compiler**: In this course, you explore the features of Encounter RTL Compiler with global synthesis technology. You learn several techniques to constrain designs, run static timing analysis, evaluate datapath logic, optimize for low power, and interface with other tools.

**Low-Power Synthesis Flow with Encounter RTL Compiler**: In this course, you use Encounter RTL Compiler with global synthesis to lower power consumption through single-pass multi-Vth optimization, hierarchical and multi-stage clock gating, multi-supply voltage (MSV) support, power shutoff, and state-retention power gating.

**Test Synthesis Using Encounter RTL Compiler**: In this course, you learn to use Encounter RTL Compiler to insert test structures in your design, synthesize for test, and connect scan chains.

**Encounter Test Jump Start to ATPG**: In this course, you learn to use Encounter True-Time ATPG for static automatic test pattern generation.

**Advanced Synthesis with Encounter RTL Compiler**: In this course, you use Encounter RTL Compiler global synthesis to debug problems in the synthesis of complex designs when optimizing for timing, area, and power.

### Place and Route

**Encounter Digital Implementation (Flat)**: In this course, you explore high-level design planning and implementation by using Encounter Digital Implementation (EDI) system software. You will learn several techniques for floorplanning, placement, detail routing, and optimization while implementing timing closure strategies.
Encounter Digital Implementation (Hierarchical): In this course, you explore the features of EDI system software for creating and implementing a hierarchical design.

Low-Power Flow with Encounter Digital Implementation: In this course, you implement several low-power techniques to reduce both dynamic and leakage power during implementation.

Prototyping and Partitioning with First Encounter: In this course, you explore high-level design planning and prototyping using the First Encounter® software. You learn several techniques for floorplanning and placement while implementing clock-tree synthesis.

Analog-on-Top Mixed-Signal Implementation: In this course you learn an in-depth approach to implementing an analog and digital mixed-signal design. You use Virtuoso Layout XL/GXL, EDI System software, NanoRoute™ router, and Virtuoso Space-Based Router (VSR) for primary and assembly routing.

Digital Implementation Basics for Analog/Mixed-Signal Designs: In this course, you learn the basics of digital implementation for analog/mixed-signal designs by using EDI System software. You explore floorplanning, placement, power planning, clock-tree synthesis, timing optimization, and detail routing.

Design Verification

Logic Equivalence Checking with Encounter Conformal EC: In this course, you use the Encounter Conformal® Equivalence Checker to perform functional verification. You learn the basic flow of equivalence checking and how to run hierarchical comparison of designs.

Encounter Conformal Constraint Designer: In this course, you use Encounter Conformal Constraint Designer to manage constraints for complex SoC designs from RTL through layout.

Low-Power Verification with Encounter Conformal Low Power: In this course, you learn to verify low-power designs using Encounter Conformal Low Power.

Encounter Conformal ECO: In this course, you learn how to implement functional ECO analysis and generation, design netlist modification, clock domain synchronization, and semantics checks by using the Encounter Conformal ECO Designer tool.

"I was very content with the training and the trainer and learned a lot which I could already implement in my work. The training will help me to efficiently develop and verify constraints of our IP in the future."

– Henrik Hostalka, Texas Instruments
Tensilica IP

Learning Map

Baseband
- Tensilica ConnX BBE64EP Baseband Engine (2)
- Tensilica ConnX BBE16 Baseband Engine (2)
- Tensilica ConnX BBE32EP Baseband Engine (2)

Audio
- Tensilica HiFi 3 Audio Engine ISA (1)
- Tensilica HiFi 2EP/Mini Audio Engine ISA (1)
- Tensilica Audio Codec API (1/2 day)

Imaging/Video
- Tensilica IVP Imaging/Video Processor (1)

See online course catalog at [www.cadence.com/training](http://www.cadence.com/training) for a complete listing of current courses.

Course Descriptions

**Tensilica Processor Fundamentals**
This two-day course provides basic information about Tensilica processor technology and how to use Tensilica’s product deliverables for your SoC design. Topics in processor architecture are discussed, and the configurable options of the Xtensa® LX series processors are outlined. You will practice working with the Xplorer Integrated Development Environment (IDE), working with Tensilica software tools, and programming Xtensa processors in the four lab exercises that are part of this course.

**Tensilica DSP Courses**
Training is available for several Tensilica DSP processor cores that are optimized for audio, baseband and imaging/video applications respectively. The HiFi family of DSPs are optimized for audio signal processing, the ConnX family of DSPs are optimized for baseband signal processing and the IVP DSP is optimized for imaging/video signal processing as illustrated in the learning map above.

The training class for each DSP provides an overview of the architecture and the instruction set of the DSP. The class covers the programming model in detail, teaching you how to write and optimize C code for the DSP. Most of these DSPs include specialized instructions relevant to the application domain, and these are illustrated in the training class. Demonstrations and labs used in the class will give you practical and hands-on experience in programming the DSP. The training class for the vector DSPs also teach techniques for programming VLIW/SIMD machines, and teach you how to write C code that can be vectorized by the C/C++ compiler.

Each training class provides the software developer or firmware engineer the essential skills necessary to develop and optimize code for a particular DSP. For more details on each class, please refer to the course description on the online course catalog at [www.cadence.com/training](http://www.cadence.com/training).

**Specialized Courses**
**Tensilica Instruction Extension Language:** This course covers how to create processor extensions that improve processing performance as well as data bandwidth for your application code. The class also teaches basic optimization and estimation techniques. Five labs covering different topics will provide hands-on experience in writing TIE code.

**Introduction to System Modeling with Tensilica Processor Cores:** This course teaches the basics of creating, configuring, and debugging a system model using the Xtensa SystemC library. Components in the XTSC example component library are described, which are used to model key components in a SoC, like cores, memories, interconnects, DMA, and others. System control, data movement, and synchronization mechanisms, like DMA transfer, GPIO interrupts, and spinlocks are also covered.