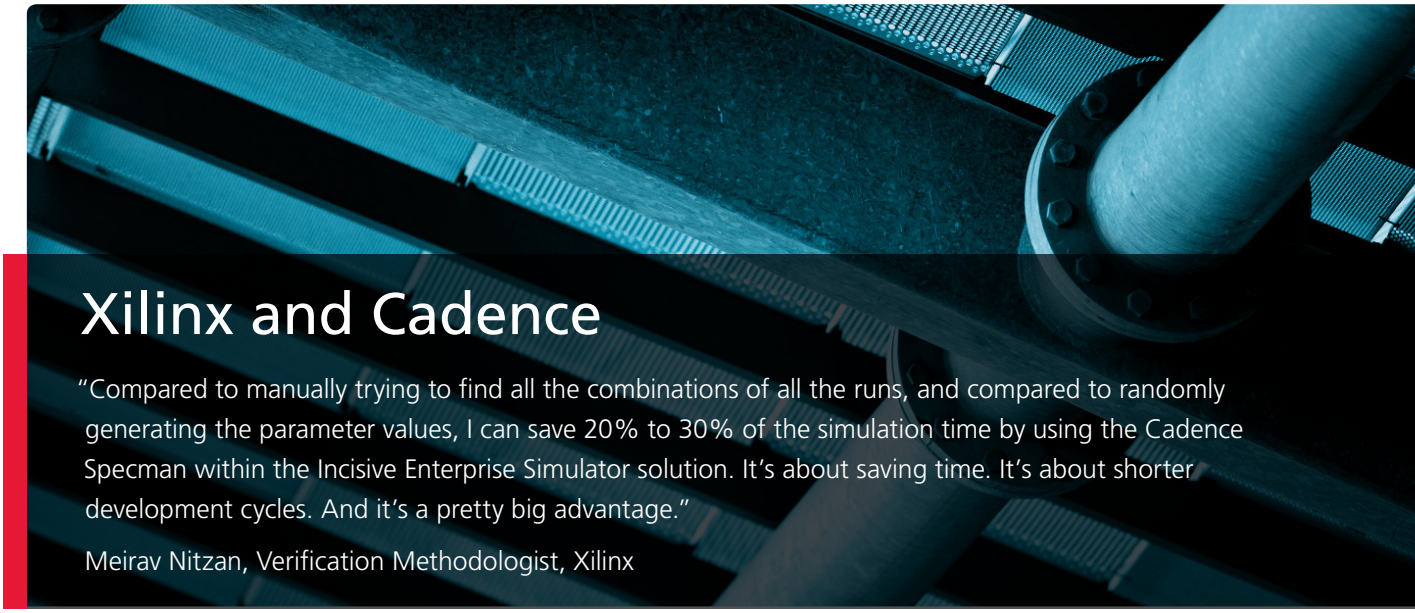
cadence®



Xilinx and Cadence

"Compared to manually trying to find all the combinations of all the runs, and compared to randomly generating the parameter values, I can save 20% to 30% of the simulation time by using the Cadence Specman within the Incisive Enterprise Simulator solution. It's about saving time. It's about shorter development cycles. And it's a pretty big advantage."

Meirav Nitzan, Verification Methodologist, Xilinx

The Customer

A leading FPGA provider, Xilinx offers customers a variety of soft IP cores to build into their designs, as well as hard IP blocks implemented in silicon during fabrication, to accelerate the development process through IP use and reuse. This rich set of IP cores represents hundreds of communications standards, memory interfaces, DSP functions, floating point operators, interconnects, and even CPUs. To facilitate customer design customization for specific end applications, Xilinx IP solutions provide many user-configurable attributes.

The Challenge

Design attributes, or parameters, affect the way any given design is going to behave, meaning that Xilinx must test its IP designs with all relevant combinations of parameter values. This is an exhaustive process during which all major design modes with all possible data-width values must be tested.

"There are many parameters for setting up the cores, and we need to verify each combination of those parameters to make sure we can deliver functionality for whatever configuration our customers need," explains Meirav Nitzan, Verification Methodologist at Xilinx.

The conventional solution is to create an exhaustive permutation set of all parameters, defined in a file that is consumed by a regression run script. This approach, however, has a number of limitations. For a design with 20 or 30 parameters, each parameter having anywhere from 2 to 10 values, there could be hundreds of thousands of combinations in the permutation set. For more complex designs, covering all the permutations might not be feasible. In either case, the turnaround time for running a regression would be prohibitively long. And there is simply no functional justification to cross check all values of all parameters with each other.

Business Challenges

- Shrink turnaround time for IP design testing

Design Challenges

- Accommodate designs with multiple, multi-value parameters
- Eliminate parameter set repetition
- Avoid redundant test suite regressions

Cadence Solutions

- Cadence Specman within the Incisive Enterprise Simulator

Results

- Enhanced parameter generation with support for both exhaustive and randomized sets
- Reduced simulation runtimes by 20% to 30%
- Increased productivity for hard and soft IP development
- Greater overall IP quality

"We try to test only the meaningful combinations," Nitzan says. "Otherwise the combination of parameters and values could be in the millions. Furthermore, when a small change is made, our verification engineers don't want to have to run a full parameter set to re-verify the core—a process that could involve a week of simulation runs."

Xilinx ultimately wanted to run a smaller set with only those parameters affected by a given change. To reach its goal, Xilinx needed the ability to randomly generate parameter sets with a solution that automatically considered the legal values of all parameters and the dependencies between parameters, avoiding parameter set repetition as well as redundant duplication of test suite regressions. The solution also had to be flexible enough to define full parameter set generation as well as smaller parameter sets to accommodate nightly regressions, specific feature testing, and other use cases.

The Solution

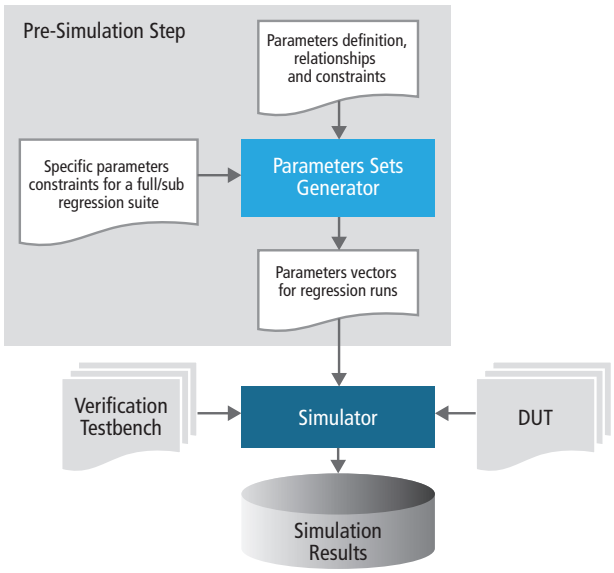
To accelerate their development cycle, Xilinx incorporated Cadence® Incisive® Enterprise Simulator with Specman® macros for enhanced parameter generation, a pre-simulation step that is now part of their regression flow. Cadence provided the Xilinx verification team with a macro for specifying which parameter sets need to be exhaustively generated (i.e. all the combinations of their values), and which fields can be simply randomized, with as little repetition as possible. The macro is built on top of the Specman ***e*** language.

"When we randomize, every repetition of values translates into another simulation run. The Cadence macro helps us avoid repetition," Nitzan says. "It gives us randomized values with almost no repetitions."

The Cadence solution yields several advantages. First, it meets Xilinx's demand for a flexible solution by enabling easy layering of constraints thanks to the aspect-oriented programming (AOP) approach used by the ***e*** language. Second, the Cadence solution enables explicit generation of exhaustive sets, while other parameters are randomly generated without repetition. Finally, Xilinx incurs no additional cost as all Incisive Enterprise Simulator licenses contain a Specman license.

Xilinx also gains ease of use and runtime improvements as a result of using the Specman solution. Regarding usability, an end user only needs to specify the parameter values and constraints, which requires very little knowledge of ***e***. Porting SystemVerilog code to ***e*** is easy, and using the new solution is simple and intuitive overall.

The runtime improvements have been dramatic. In the past, Xilinx mainly used Perl scripts to generate parameters, which worked fine for small parameter sets but quickly became unmanageable for regressions involving a high number of parameters, each with several possible values. Creating an exhaustive cross check of all



possible parameter values required checking the generated values to ensure no repetition, but that process could easily take more than an hour to run and could choke the computer.

Xilinx had also tried to solve its runtime problem using SystemVerilog randomization via the simulator. But this offered no guarantee that the values generated were free of repetitions. Every repetition means a redundant simulation run that can take a few seconds to several minutes.

"Compared to manually trying to find all the combinations of all the runs, and compared to randomly generating the parameter values, I can save 20% to 30% of the simulation time by using the Cadence Specman within the Incisive Enterprise Simulator," Nitzan said. "It's about saving time. It's about shorter development cycles. And it's a pretty big advantage."

Summary and Future Plans

Incisive Enterprise Simulator with Specman technology provides Xilinx increased productivity for both hard and soft IP development, and it improves overall IP quality. Several cores have already been using the attribute generation solution in their regression successfully. Xilinx has recently released an internal regression management tool which uses this solution, and plans to deploy it on all silicon IP teams.

"Managing simulation regressions of highly parameterized designs is a difficult challenge. Specman technology with the added macro solution, which was adapted to our needs, makes a huge difference in our ability to handle this challenge. Moreover, Cadence has shown resourcefulness and a high level of responsiveness during the development of this solution," Nitzan concludes.