cadence®

Xcelium Parallel Logic Simulation

Breaking through functional verification bottlenecks provides highest productivity for your most complex IP and largest SoC projects

Cadence® Xcelium™ Parallel Logic Simulation is the third generation of digital simulation. At its core is the first production-proven multi-core engine. Unified with that engine are the industry's fastest single-core, randomization, and mixed-signal engines to simulate all use cases, and supported by second-generation simulators. Enabling these use cases are the most comprehensive set of language, methodology, power, coverage, and functional-safety technologies. The Xcelium simulator runs on your existing compute resources with leading runtime and capacity, making it the simulator of choice throughout the verification flow.

Introduction

As system-on-chip (SoC) designs have grown in size, simulation technologies have had to evolve dramatically to keep pace. The first generation of commercial simulation technology emerged in the late 1980s and was marked by interpreted-code simulators such as Verilog-XL and RapidSim. Since such simulators compiled to a form of p-code and then interpreted that code, they ran rather slowly, but were suited to the smaller designs of the time.

Next came compiled-code simulators in the mid-1990s, providing the speed and capacity for designs that quickly grew larger with the emergence of synthesis. Compiled-code simulators convert source code into machine code before running the simulation. These second-generation technologies were more complex to build, taking about three years to implement simulation for the existing languages and use models at that time. Since then, they have served the industry quite well, implementing a wide range of new standards including ***e***, SystemC®, SystemVerilog, CPF, and UPF. But now, designs are growing even larger and more complex.

Xcelium Parallel Logic Simulation launches the third generation of simulation. It provides multi-core speed-up for RTL, zero-delay gate-level, and zero-delay design for test (DFT) use cases, and single-core support for all other use cases currently running on second-generation simulations, including the Universal Verification Methodology's (UVM) testbench, low-power, mixed-signal gate simulation with Standard Delay Format (SDF) timing and more. Many of these use cases will have multi-core support in the future. The Xcelium simulator automatically partitions the accelerate-able portions across multiple cores on your existing server farm resources and allows you to continue using your familiar verification environment, methodologies, and debug without change while accelerating runtimes by 3X-10X on average. The Xcelium simulator is the simulator of choice throughout the verification flow.

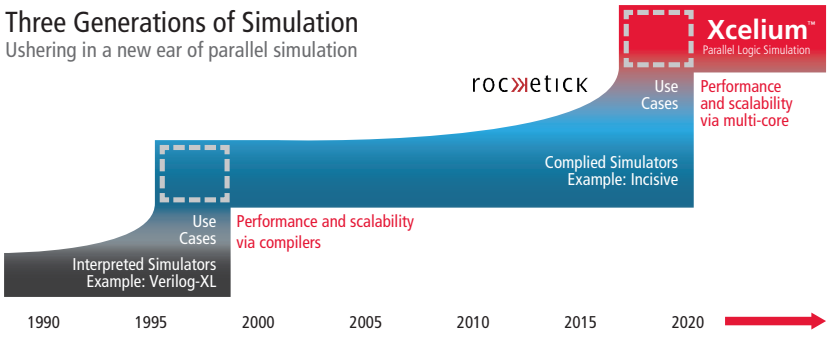

Figure 1: The Xcelium simulator launches the third generation of simulation, unique multi-core parallelism breaks SoC-level bottlenecks.

Key Benefits

- Largest capacity and fastest runtime for SoC-level tests
- Fast IP-level tests driven by ***e***, SystemVerilog/UVM, SystemC, and other languages
- Seamless single-core to multi-core integration
- Auto-partitioning of accelerate-able design and non-accelerate-able partitions
- Multi-core parallelism regardless of design topology, structure, or hierarchy
- Fully supports low power, X-propagation, and mixed signal
- Unified coverage database integrates simulation, formal, acceleration, software, fault, and use case coverage
- Enables unified debug for all use cases including interactive and batch debug

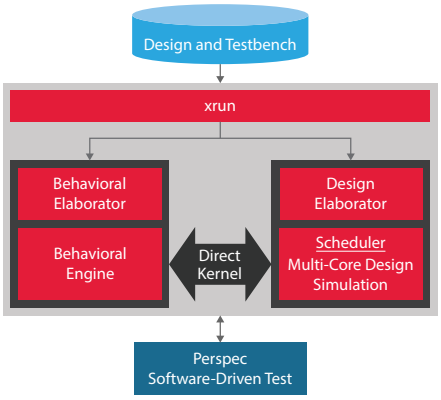

Figure 2: The Xcelium simulator 's partitioning of accelerate-able design and non-accelerate-able partitions

High-Performance Simulation

The definition of the third-generation simulator is the combination of significant speed-up and simulation automation. The Xcelium simulator delivers both. It analyzes the entire design with its testbench, partitioning the accelerate-able code to the multi-core engine and non-accelerate-able code to the single-core engine. At this time, it identifies the complex dependency maps at a fine-grained design level. This resulting set of many millions of truly independent event-chains are mapped over available cores to run independently in parallel and scheduled to communicate with the single-core engine.

This approach defines a third-generation engine opening the door for verification engineers to more actively stimulate their designs. Active stimulus creates more events in each simulation run that is needed to model the actual functionality in modern designs. Since third-generation simulators are able to distribute the extra activity to parallel cores, it provides both a speed and verification quality advantage over second-generation simulators. In this way, the Xcelium simulator provides 3X to 10X performance gains for SoC designs.

Performance benefits of the Xcelium simulator's multi-core parallelism include:

- Simulation acceleration on average 3X – register transfer level (RTL), 5X – gate-level simulation (GLS), and 10X - GLS-DFT: Expand your simulation capacity, and reduce hour-long RTL runs to minutes and multi-week DFT runs to days
- Automatic partitioning: Enables multi-core, parallel build, and multi-core speed-up for the largest SoC designs with no learning curve
- Multi-core parallelism at the fine-grain design level: Multi-core speed-up unaffected by design type, structure, hierarchy, or process node
- Runtime mapping onto the industry's available standard multi-core servers: Use existing X-86 servers
- Compatible with your existing environments, verification method-ologies, and interactive debug processes: Move between single-core and multi-core engines without code changes or environment restrictions

The Xcelium simulator provides parallelism with multi-core speed-up, benefiting event-dense simulation runs of all types.

Additional Parallelism

The Xcelium simulator also takes advantage of parallelism for additional verification processes. These tasks can be performed in parallel on different cores or even different machines across a network, and results can be assembled post-process without noticeably degrading performance.

The Xcelium simulator's tasks that can run in parallel include monolithic elaboration, code generation, and two modes of multi-snapshot incremental elaboration (MSIE), providing better user control and superior performance. Single-run auto-MSIE allows command-line primary and incremental partitions to be defined to gain up to 10X build improvement. Multi-run MSIE allows users to more directly control elaboration partitioning for much greater storage and runtime savings. More importantly, MSIE allows tighter control over re-use and environment consistency. This ensures verification teams located across regions and time zones are all working from the same consistent primary base as they optimize and debug their changing incre-mental DUT partitions. Each incremental iteration needs far less memory and shorter runtime.

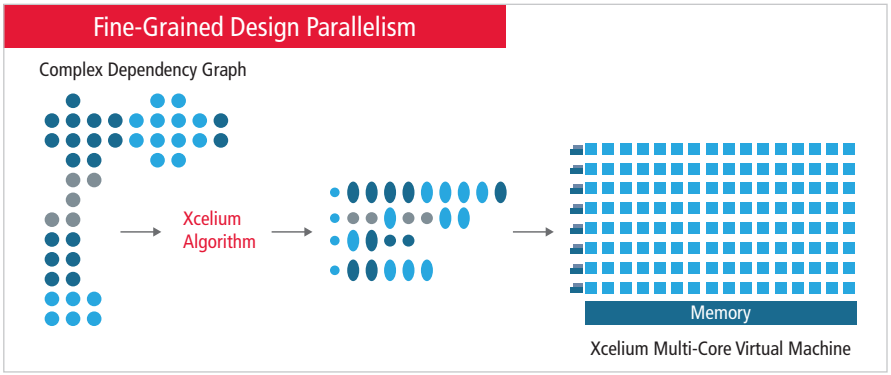

Figure 3: The Xcelium simulator's complex dependency graph technology enables multi-core parallelism

Additional parallelism in the Xcelium simulator includes:

- Compile and elaboration partitioning
  - Monolithic elaboration code generation – up to 1.5X improvement
  - MSIE automated – up to 10X build time and storage improvements
  - MSIE multi-run – up to 20X or more, creating re-useable, deployable, and stable primary partitions
- Save and restore and dynamic restart
- Debug dumping for 2X runtime and peak memory reduction
- The Cadence Integrated Metrics Center (IMC)'s individual-test coverage merge and ranking to multiple cores with 3X on four cores observed
- The Cadence vManager™ Metric-Driven Signoff Platform's multiple-regression coverage merge and ranking, linear with number of cores with 4X on four cores observed

Testbench Performance, Coverage, and Debug

Meeting your verification goals depends on your testbench and verification methodology. Regression coverage metrics, interactive debug, long, deep corner case bugs, functional safety faults, low-power modes with initialization, and digital interfaces with analog and mixed-signal boundaries are essential challenges for SoC verification.

Cadence led the development of UVM by providing methodology and code from OVM and building on eRM. UVM, including the IEEE 1800.2 standard, is supported in the Xcelium simulator for SystemVerilog, ***e***, and SystemC. In addition, the Xcelium simulator supports the emerging Accellera standard for multi-language UVM.

But how do you recognize whether the testbench is exercising the design as intended? The Xcelium simulator's testbench coverage capability provides metric-based reporting of testbench activity, ensuring you know of untested parts of your design by identifying portions of the testbench that have not been appropriately active. Likewise, when a simulation fails, is it a design or testbench issue? Combining the Xcelium simulator's native linting for ***e***, SystemVerilog, and RTL with testing features and with the Cadence Indago™ Debug Analyzer, you can more fully develop, test, and debug to create the most effective testbenches possible.

Inseparable Low-Power and Reset Verification

The simulation burden has exploded with smaller geometries requiring many tens to hundreds of power domains operating at various different voltage levels and controlled by embedded software. Consistency between simulation, formal, and emulation views is essential for your verification team.

The Xcelium simulator's low-power simulation brings comprehensive IEEE 1801 (UPF) and CPF support. Cadence pioneered using native engines to allow all low-power information to be analyzed once during elaboration, instead of during each simulation run, for lower overhead and cleaner integration, meaning every simulation can be power aware. The same power intent can be carried through from architectural abstraction through design implementation and all CPF/UPF objects including CPF power-modes and UPF power-states can be checked to compare isolation, state retention, and state loss actual behavior against the expectation for post synthesis and post place-and-route implementations. Verification of shutoff and restore behavior can be accomplished at the design level, for the logical netlist, and through to physical implementation.

Integration with Cadence Conformal® Low Power and with the Cadence JasperGold® Low-Power Verification (LPV) App enables power intent equivalency checking, and Xcelium simulation allows final verification at the SoC level to ensure the scan and other physical structures inserted have not altered your power intent.

Power-up reset, initialization, and corruption recovery are critical to low-power behavior. The Xcelium simulator's X-propagation support verifies reset and initialization and allows you to dynamically choose the appropriate level of pessimism or optimism for each section on a design/level/block/instance basis using the X-propagation tools during simulation of VHDL and SystemVerilog. The Xcelium simulator's native CPF and UPF support work together with X-propagation to verify that retention and

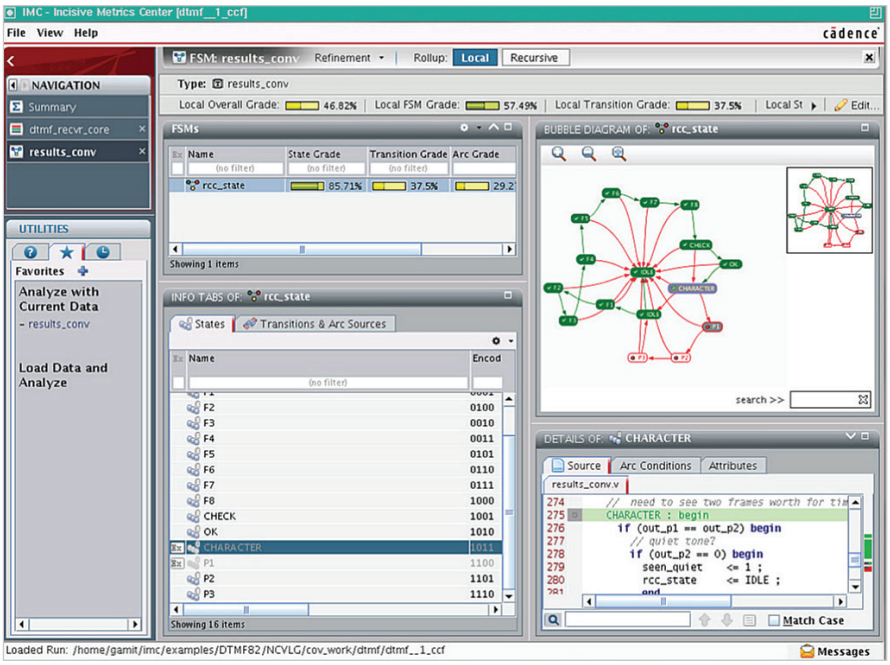

Figure 4: The Xcelium simulator provides the Cadence IMC for concurrent dynamic analysis views. Shown here: Context-aware activity for finite state machine analysis.

isolation corruption follows power intent and will recover correctly from low-power modes.

The Xcelium simulator provides the IMC to measure coverage on low-power objects, power-modes, and power-states. The Cadence SimVision™ Debug platform delivers waveform, schematic, and power supply network browser features to visualize and debug all aspects of power intent. Reset and initialization verification using X-propagation helps fully ensure each power domain of the design cleanly recovers from power-down corruption schemes.

Analog Mixed-Signal and Digital Mixed-Signal Simulation

The Xcelium simulator is integrated with the Cadence Spectre® Circuit Simulation Platform for analog mixed-signal simulation. Users of this flow typically capture a design and testbench in the Cadence Virtuoso® Analog Design Environment and netlist it to run with the Xcelium simulator and a Spectre engine. The Xcelium simulator provides the xrun unified front end to compile and elaborate the netlist for simulation. In this use model, the analog engines are simulating at transistor level, Verilog-AMS, or VHDL-AMS, and may include WREAL modeling within the AMS languages for both power-managed and non-power-managed tests.

The Xcelium simulator can also simulate high-speed digital mixed-signal models. These models are typically written with SystemVerilog real number modeling (RNM), Specman Elite, or VHDL. These models provide high accuracy and support randomization and functional coverage, enabling digital mixed-signal simulations to run at digital speeds. As with multi-core engines, this support allows SoC feature testing that can't be done by traditional mixed-signal approaches for both power-managed and non-power-managed tests.

Coverage and Randomization Performance

Randomization performance is critical to achieving functional coverage in the shortest number of cycles, finding more bugs faster. The Specman/***e***-based Inteligen engine inspired the Xcelium simulator's new Xceligen randomization engine. The Xcelligen engine manages multiple new solvers, automatically choosing the most appropriate solver for the task. The Xcelium simulator's randomization performance is up to 5X faster than in previous simulations.

Analyzing metrics is a critical part of any functional verification flow. The IMC provides a single, integrated portal for viewing and analyzing the vast array of metrics and coverage data generated within the verification platform. The IMC enables context-aware activity centers, dynamic user interactivity, deep-dive coverage analysis, and high-performance merging and ranking to help you refine your regression runs. Intuitive and easy to use, the IMC greatly improves verification productivity at every stage of the flow.

The results from all this advanced technology are pulled together and either executed or collected by the vManager platform. The vManager platform, and the IMC embedded within it, provides a powerful, customizable, project-level view of verification that is specifically tailored and optimized to the Xcelium simulator, bringing visibility and efficiency needed for effective verification planning and to manage and accelerate coverage closure for small to multiple geography and distributed verification teams.

Gate-Level Simulation

Gate-level simulation requirements have exploded with finer process nodes, dramatically multiplying additional cell timing checks to represent more than a billion gates. The Xcelium simulator's zero-delay and unit-delay gate-level simulation speeds through functional simulations to resolve race and loop conditions, and verify functionality. This reduces SDF timing gate-level simulation to those essential checks unavailable in other engines.

For gate-level simulation with back-annotated timing, the Xcelium simulator is optimized to run your simulations faster and with less memory, using many options for timing, access, and initialization of registers to streamline your gate-level timing simulation.

Parallelism for multi-core waveform dumping, multi-snapshot incremental elaboration, and save and restart reduces setup time and preserves stable base partitions for iterative tasks, taking your simulation back to the point of interest and allowing new scenarios to run forward. The Xcelium simulator is integrated with the Cadence Palladium® platforms, allowing the design to be run at highest performance in emulation and run for debug in software simulation.

SoC Verification

Ever-growing SoC verification prompted development of high-level verification languages like ***e*** and SystemVerilog, along with companion methodologies such as the UVM. But language and methodology take you only so far.

Bugs in full-chip are few but those bugs are big misses that can escape IP and subsystem regressions. Additionally, final SoC verification requires interconnect validation, performance profiling, and physical netlist validation to ensure all IP integration and physical structures instantiated for low power control and for scan and test have not altered your design intent.

In spite of great advancements in formal, VIP, and emulation technologies, functional simulation is still required for final SoC-level verification. The Xcelium simulator unites tools to mix gate-level simulation for testing interface performance, mixed-signal and software domains, hundreds of low-power domains, and their initialization and reset behavior. The interconnect validator application helps quickly verify interconnect connectivity across all your IP boundaries and the Cadence Interconnect Workbench accelerates performance analysis and verification of on-chip interconnects throughout your SoC by identifying bottlenecks under critical traffic conditions.

Multi-snapshot incremental elaboration creates stable and reuse-able primary partitions to allow your team to focus on the portion of the design under test. Save and restart with dynamic restart

takes your simulation back to the point of interest and allows new scenarios to run forward.

The Xcelium simulator also provides the capacity and performance needed for your largest SoCs. The ability to use Xcelium simulation and Palladium emulation in a flow enables high speed for reset, asynchronous, and low-power simulation with 4-state accuracy and then higher-speed 2-state accuracy for longer tests focused on system simulation, including tests in the context of software.

The Xcelium simulator is one of the best-in-class engines within the Cadence Verification Suite. Effective use of the different engines is enabled via Cadence verification fabric technologies supporting portable stimulus, a unified plan to closure with Metric-Driven Verification (MDV), verification IP, and debug across the engines.

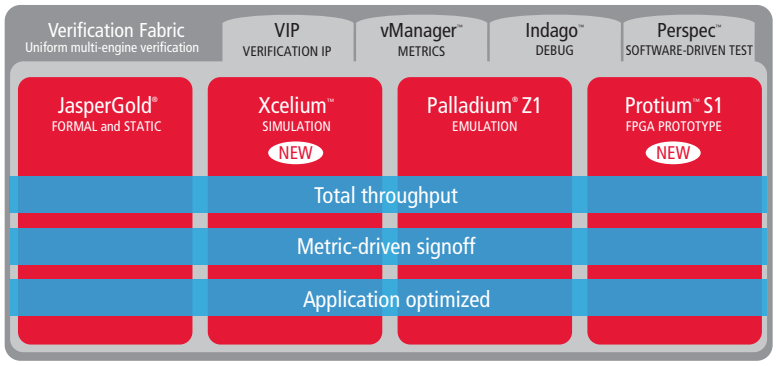

Figure 5: Cadence Verification Suite

Multi-domain debug capabilities are required for SoC verification, including core debug (RTL, gate-level, and testbench), low power, mixed-signal, embedded software, software-driven use-case, and protocol debug. The innovative SimVision and Indago debug platforms provide differentiated solutions for all of these debug requirements across the engines.

SystemVerilog and the UVM's bottom-up approach using constrained-random coverage-driven testing is not sufficient for large SoC-level verification. Real-world use cases that work are necessary for both vertical (IP to SoC) and horizontal cross-platform re-use, supporting the entire workflow from architectural evaluation through emulation for software application testing. The Cadence Perspec™ System Verifier automates the creation of software-driven real-world use-cases to address this challenge. The Perspec System Verifier's development is helping advance the Accellera portable stimulus working group standard.

It's becoming more common for specifications for standard interface protocols to be hundreds of pages long. Deciphering these specs and accurately modeling the protocols is a big development effort requiring deep technical knowledge. By using production-proven Cadence Verification IP (VIP), you can verify your SoC designs faster, more thoroughly, and with less effort. Cadence is the industry VIP leader with products supporting more than 40 communication protocols and 60 memory interfaces.

You also have the freedom to build your custom VIP testbench using any of these verification languages: SystemVerilog, ***e***, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports UVM as well as other methodologies.

The unique and flexible architecture of Cadence VIP makes all this possible. It includes a multi-language testbench interface with full access to the source code making it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Unified Plan to Closure with MDV

You can use the integrated multi-window GUI with the vManager platform to drive the verification process right from the planning stage. Following the guidelines of the MDV methodology, verification teams can automatically capture the verification objectives from the written verification plan, create a vPlan executable specification, and automatically compare and communicate progress against the vPlan.

Both the Xcelium simulator and Palladium platforms produce coverage data at the end of execution by writing out coverage results into a unified coverage database (UNICOV), consistent with the MDV methodology and integrated with the vManager platform for easy adoption. The vManager platform provides a powerful, customizable, project-level view for verification that is specifically tailored and

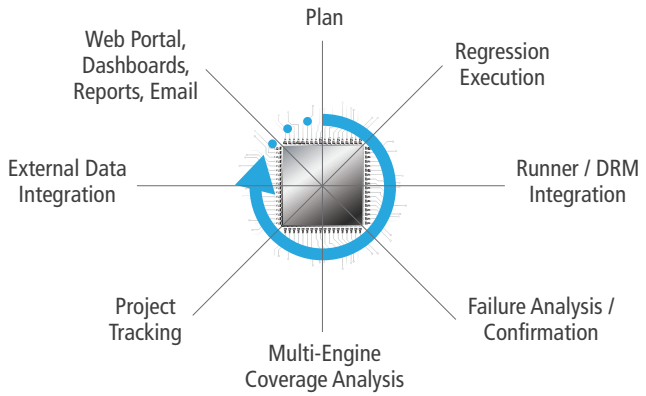

Figure 6: The vManager platform's advanced verification methodology control cycle

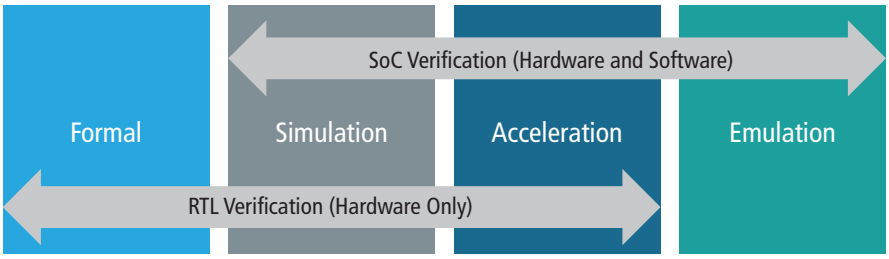

Figure 7: The Xcelium simulator and vManager platform take metric-driven verification further with multi-engine MDV methodology

optimized for the Xcelium simulator. The vManager platform takes MDV beyond the industry-leading IMC, to execute tests across the server farm, collect test results, combine coverage results, and create a verification plan, and it will do so with the Xcelium simulator, JasperGold Formal Property Verification (FPV) App, and Palladium platform. The vManager platform is also used to execute and collect results from the Xcelium simulator, and with the Perspec System Verifier. The vManager platform is a fully customizable planning and management tool, which easily connects to your customer's enterprise applications, and includes a commercial SQL database for tracking verification progress over time.

With the vManager platform and Xcelium simulator, Cadence takes the MDV methodology beyond traditional RTL simulation-only testing. The multi-engine MDV methodology allows users to take the best tool for the job and combine results transparently. The Perspec System Verifier's random stimulus generation runs on the Xcelium simulator and Palladium platform, and is used for top-down software-driven testing to ensure all use cases are covered, while simultaneously reading back which parts of the RTL were covered by those software tests. The JasperGold FPV App is a simple and easy adaptation to traditional simulation-oriented flows, with push-button automation for verification tasks such as connectivity checking, register checking, and X-propagation. Coverage unreachability is another fully automated application deeply embedded into the vManager platform and the Xcelium simulator, making coverage closure faster. For teams looking for more, the JasperGold FPV App with coverage allows advanced bug-hunting techniques that nicely complement the Xcelium simulator, with easily combined data results to show productivity levels by engine.

Features and Benefits

- Speeds up RTL, gate-level, and gate-level DFT functional simulations for higher productivity
- Provides over one billion logic gate capacity for full SoC-level simulation
- Automated multi-core partitioning supports existing environment and tools for quick ramp-up
- Runs on standard multi-core servers in existing server farms
- Scales to available cores for higher performance
- Accelerates design code on multiple cores alongside the testbench without altering your environment
- Complies with IEEE 1364 Verilog, IEEE 1800 SystemVerilog (including SVA), IEEE 1801 UPF, IEEE 1076 VHDL, IEEE 1647 Specman/***e***, IEEE 1666 SystemC, IEEE 1735 IP Protection,
- Executes full support for four-state logic (0, 1, X, Z) in all modes
- Supports mixed signal, low power, X-propagation, and debug across other verification technologies and flows
- Supports UVM, eRM, and OVM testbench methodologies
- Supports PLI/VPI-compliant interface
- Provides full debug visibility in interactive and post-process use cases
- Supports standard debug tools including direct dump of waveforms

Cadence simulation has always provided the most integrated unified verification with the widest support for standard languages, methodologies, and flows. With the Xcelium simulator and its third-generation multi-core parallel simulation your verification schedule is no longer at the mercy of simulation bottlenecks. Cadence support is unexcelled as a partner to keep your unique verification project on schedule.

Specifications

- Comprehensive language support
  - Verilog (IEEE 1364)
  - SystemVerilog (IEEE 1800) including SVA
  - ***e*** (IEEE 1647)
  - VHDL (IEEE 1076)
  - SystemC (IEEE 1666)
  - PSL (IEEE 1850)
  - UPF (IEEE 1801)
  - Silicon Integration Initiative (Si2) Common Power Format (CPF)
  - 1735-2014 – IEEE recommended practice for encryption of IP
- Code coverage
  - Supports Verilog, SystemVerilog, VHDL, and mixed-language designs
  - Automatic finite state machine extraction
  - Coverage attributes supported include blocks, paths, expressions, variables, gates, FSM (states, sequences), and toggle
  - Coverage waiver (refinement) reuse
  - Rank order coverage contributions
  - Bit-wise expression scoring
- Functional coverage analysis
  - Supports Verilog, SystemVerilog, VHDL, ***e***, SystemC, SCV, PSL, SVA, and OVL
- Cadence SoC Functional Verification Kit
- Verification IP
  - Supports the full portfolio of Cadence Universal Verification Components (UVCs): PCI Express® (PCIe®), AHB, AXI, USB, and Ethernet, PCI, SATA, and OCP
  - Supports all simulation-based UVCs, transaction-based VIP, assertion-based VIP, and Cadence SpeedBridge® interface rate adapters used in emulation
  - UVCs are designed to use all elements of Cadence Incisive® Enterprise Simulator, featuring a comprehensive Compliance Management System that leverages vPlans to exhaustively verify protocol compliance

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the exibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training

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