cadence®

Virtual Debug Interface to Software Debuggers

Processor debug with industry-standard debuggers

The Cadence® Virtual Debug Interface to Software Debuggers provides a "virtualized" interface between Cadence's Palladium® Verification Computing Platform and a software debugger, enabling designers to remotely debug processors with either JTAG, DAP, or Arm® AMBA® APB or AHB bus interfaces. This complements the physical debug interface, offering connectivity options to engineers.

Overview

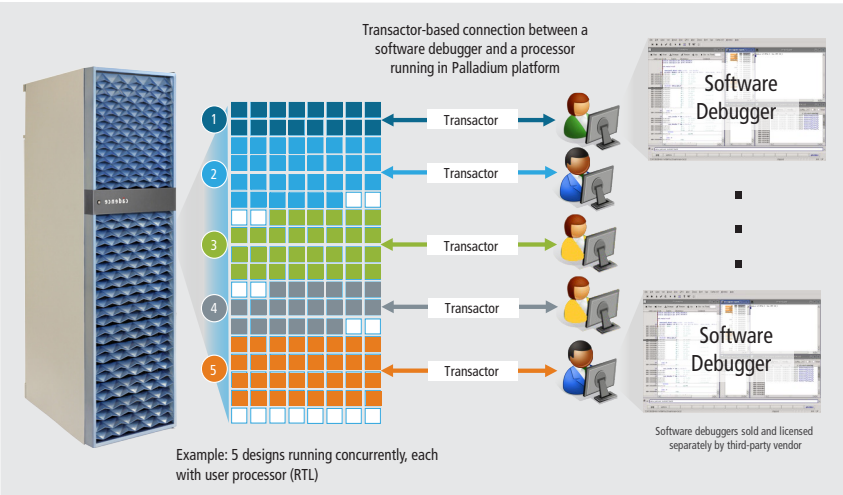
In order to perform hardware/software co-verification, software engineers require access to processors emulated in the Palladium series platform. Most processors provide on-chip debug access via a JTAG connection scheme. JTAG is an IEEE 1149.1-1990 standard for on-chip instrumentation using a dedicated serial communications interface for low-overhead access.

Some processors can also be accessed by a system bus inside the debug subsystem, allowing much faster throughput. Interfacing to internal buses is only possible with a virtual interface, and can be used in simulation acceleration or virtual emulation use cases.

Software debuggers provide a software interface to access processors to perform debugging with capabilities such as single-step, read/write memory, read/write CPU registers, set breakpoints, and triggering.

Virtual Debug Interface to Software Debuggers

The Virtual Debug Interface provides a connection between the software debugger using its software interface and the emulated processor core, enabling software designers to inter-



Virtual Debug Interface

JTAG or APB / AHB or DAP

Benefits

- Remote access designs in any hardware domain(s)
- Specialized hardware accessory is not required
- Enables more software engineers to debug their designs

Figure 1: Enabling multiple software engineers to debug concurrently with virtual debug interface

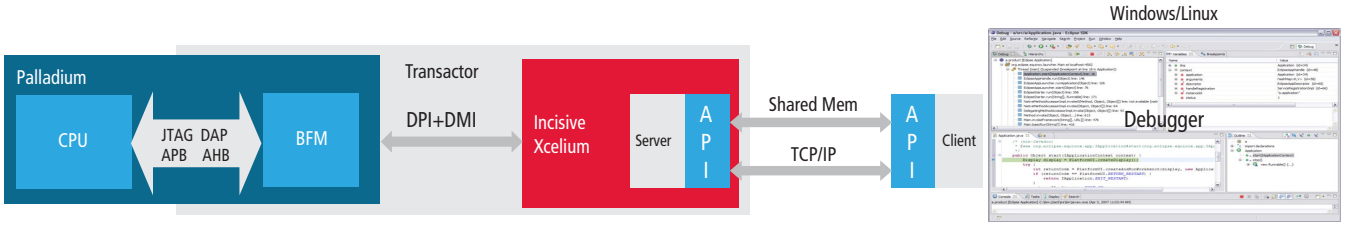


Figure 2: Block diagram overview of virtual debug interface

actively and remotely debug the software running on one or more processors. The connection does not require any hardware probes or cables—it is "virtualized".

The Virtual Debug Interface supports either a serial, such as JTAG, or parallel signal-level protocol to access the emulated processor. A parallel protocol, such as the AMBA APB offers significant improvement of access times over JTAG.

Benefits

- Higher performance option than JTAG
- Access designs in any hardware domain
- No PODs needed for JTAG or bus access
- Remotely accessible—connect from any remote workstation
- Enables more software engineers to debug their designs remotely

Features

- Soft (virtual) debug interface from JTAG, AMBA APB, AMBA AHB, or DAP bus-compatible processor running in Palladium Verification Computing Platform to Lauterbach Trace32 debugger
- Supports Palladium XP, XPII, and Z1 platforms
- Supports Transaction-Based Acceleration (TBA), Virtual Emulation, and In-Circuit Acceleration modes

Software Support

- Cadence Verification Xcellerator Emulator (VXE)
- Cadence Xcelium™ Simulator
- Debugger: Lauterbach Trace32, Arm Development Studio, Cadence Xtensa® OCD

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or internet. They can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24×7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more.
- For more information, please visit www.cadence.com/support and www.cadence.com/training for training.

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