

# Specman Elite Offers Vast Flexibility to Developers

## Valens and Cadence

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### The Customer and Service Provider

Valens Semiconductor is an Israeli Fabless manufacturing company providing semiconductor solutions for the development of HDBaseT (HDBT) devices. This technology, invented by Valens, is used for transmitting uncompressed high-quality images and audio from the basestations, potentially up to 100 meters (328 ft) through a single cable, to remote displays as a part of its 5Play system. HDBT is transmitted over category 6a cables with 8P8C modular connectors of the type commonly used for Ethernet local area network connections. HDBT transmits uncompressed ultra-high-definition video (up to 4K), audio, power over HDBT, Ethernet, USB, and a series of controls such as RS and IR.

HDBT is complementary to standards such as HDMI, and it is an alternative to radio frequency, coaxial cable, composite video, S-Video, SCART, component video, D-Terminal, or VGA. HDBT connects and networks devices in the audiovisual field, consumer electronics, medical and governmental applications, and in the automotive market.

Also involved with solving the challenges for designing HDBT devices was Veriest, an international design house with over 100 engineers, providing advanced ASIC and FPGA design and verification services. Veriest's mission is to provide customers with superior quality solutions suited to the various phases of a product's life cycle, including architecture design, design implementation, system integration, advanced verification, and embedded software.

### The Challenge

Today's ASIC devices deliver increasingly more complex RTL lines of code, more gates, and correspondingly more features wrapped with better efficiency. These new features represent higher logic complexity, supporting more configurations than ever before.

The project that Valens was undertaking was designing the HDBT Switch (T-switch), which has the following features:

- 16 ports with 16Gbps per port, using a non-blocking switch
- Supporting HDBT wire-speed packet switching

### Key Challenges

- A complicated 16-port with 16Gbps per port resulting in an unthinkable number of verification scenarios
- Many engineers and developers were working together, spanning teams from various countries
- The developers needed to quickly integrate engineers with different levels of knowledge

### Cadence Solution

- Cadence® Specman® Elite

### Results

- 480 tests performed with 185,000 registers in ASIC
- Macros used in about 75% of tests
- When using the `ADD_STREAM` macro, 12X fewer lines of code to verify the design
- Exhaustive coverage achieved
- Tapeout was on time

- Switching any combination of T-Adaptors / HDBT ports
- Each port supports HDCP 2.2 and HDCP 1.4
- Management over Ethernet or I2C
- ValUE management and control system

From a verification point of view, these complex ASICs imply several problems to consider when planning a verification environment; specifically, how to cover all the different configuration options, while, at the same time, meeting shortening schedule demands.

The main challenges in this project, though, were three-fold:

1. A 16-port with 16Gbps per port is complicated, with an unthinkable number of verification scenarios
2. Many developers worked together, spanning teams from various countries
3. The team needed to quickly integrate engineers with different levels of knowledge

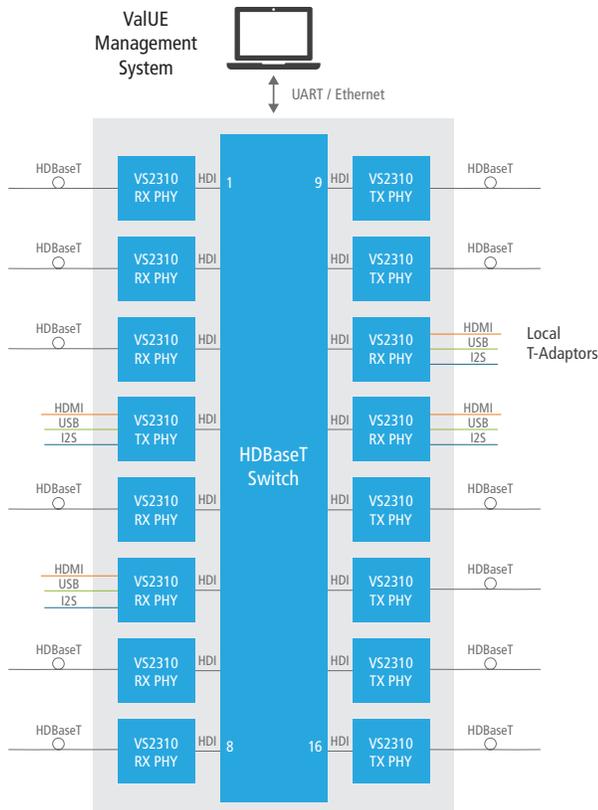


Figure 1: Native and HDBT switching

## The Solutions

To approach these challenges, the team relied on the capabilities of Cadence Specman Elite. The main reason for choosing Specman Elite over SystemVerilog is due to the aspect-oriented programming feature of Specman support, which allows a verification engineer the vast flexibility one would need to deliver desired scenarios as quickly as possible. Specman Elite is also easy to learn and maintain. The ability to add syntax (and create code that is even easier to learn and maintain)—was the deciding feature.

Specman macros define parameterized code, which is instantiated by substituting parameters. In principle, a macro is used to extend `e` and add new language constructs. In general, a macro definition specifies:

- A syntactic pattern that defines a new syntactic construct in the language
- A replacement that specifies `e` code containing other, already existing constructs of the same category

To reduce the lines of code required to verify the design, Valens employed the use of these macros.

The main usage of the macro is providing the test writers easy-to-use syntax—syntax that does not require being familiar with the language, the testbench, or the methodology. Using macros allows new and inexperienced engineers to create desired scenarios. This mechanism also allowed the chip designers to create and run simple tests for sanity checks during RTL development, without too much knowledge about the Specman code itself.

For example, the `ADD_STREAM` macro requires about 15 lines of code in most situations. This simple macro instantiation translates into 180 lines of actual code. The macro was used 16 times in one of the main verification scenarios, which translates to a 1200% decrease in lines of code for this one macro usage.

*“...By using Specman macros, we achieved higher efficiency for our verification engineers as they were able to produce test scenarios right from day one.”*

Ron Sela  
Verification Group Leader, Valens Semiconductor

## Summary Results

There are multiple advantages in implementing this kind of solution in Specman Elite. Unlike other languages, with `e` macros, the implementer decides the syntax they give their users. The macro usage does not have to look like a function call. When a macro has as many parameters as this utility requires, there is a big advantage in terms of simplicity.

Future enhancements to this utility can be to encapsulate macro within macro, to make the code even shorter and easier to maintain. Parts of the macro body that do not depend on the parameters can be cut out into another macro and conditionally called by the main macro.

Due to the implementation of using Specman Elite macros in 75% of the tests, the project taped out on time with all project goals achieved. The project spanned over 2.5 years, 14 verification engineers, 7 design engineers, 480 tests with 185,000 registers in ASIC performed, and 12X fewer lines of code required. Exhaustive coverage was achieved in an accelerated timeline, resulting in a successful design.

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