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Texas Instruments and Cadence

"We continue to improve our power expectation, power estimation, and silicon measurement for our OMAP application processor. With Cadence Palladium XP Dynamic Power Analysis, combined with Encounter Power System, we achieved greater-than 90% accurate correlation between the architects' power estimation and actual silicon power consumption measurements, enabling us to deliver the best thermal and power experience to our customers."

Norbert Isaac, Verification Engineer, Texas Instruments

The Customer

Texas Instruments (TI) develops system-on-chip (SoC)-based application processors that serve markets ranging from feature-rich phones to high-end, multimedia-rich wireless handsets.

The scalable Open Multimedia Applications Platform (OMAP) processors from TI deliver the best combination of high performance and ultra-low power consumption. The OMAP 5 platform includes applications processors featuring wireless connectivity, power management, battery management, and audio management for next-generation smartphones, tablets, and other mobile devices. The platform also features strong open-source software for faster time to market.

The OMAP platform consists of the following:

- Two ARM® Cortex™-A15 MPCore processors, each capable of speeds up to 2GHz
- Two ARM Cortex-M4 processors for low-power offload and real-time responsiveness
- Multi-core PowerVR SGX544-MPx graphics accelerators for 3D gaming and 3D user interfaces
- Dedicated TI 2D BitBlt graphics accelerator
- IVA-HD hardware accelerators enable full high-definition (HD), multi-standard video encode/decode as well as stereoscopic 3D (S3D)
- Faster, higher-quality image and video capture
- Single SoC built in 28nm process technology on a 70mm^2 die

Business Challenges

- Deliver the best application processor with optimal performance, power consumption, and thermal conditions
- Limit power consumption within two watts

Design Challenges

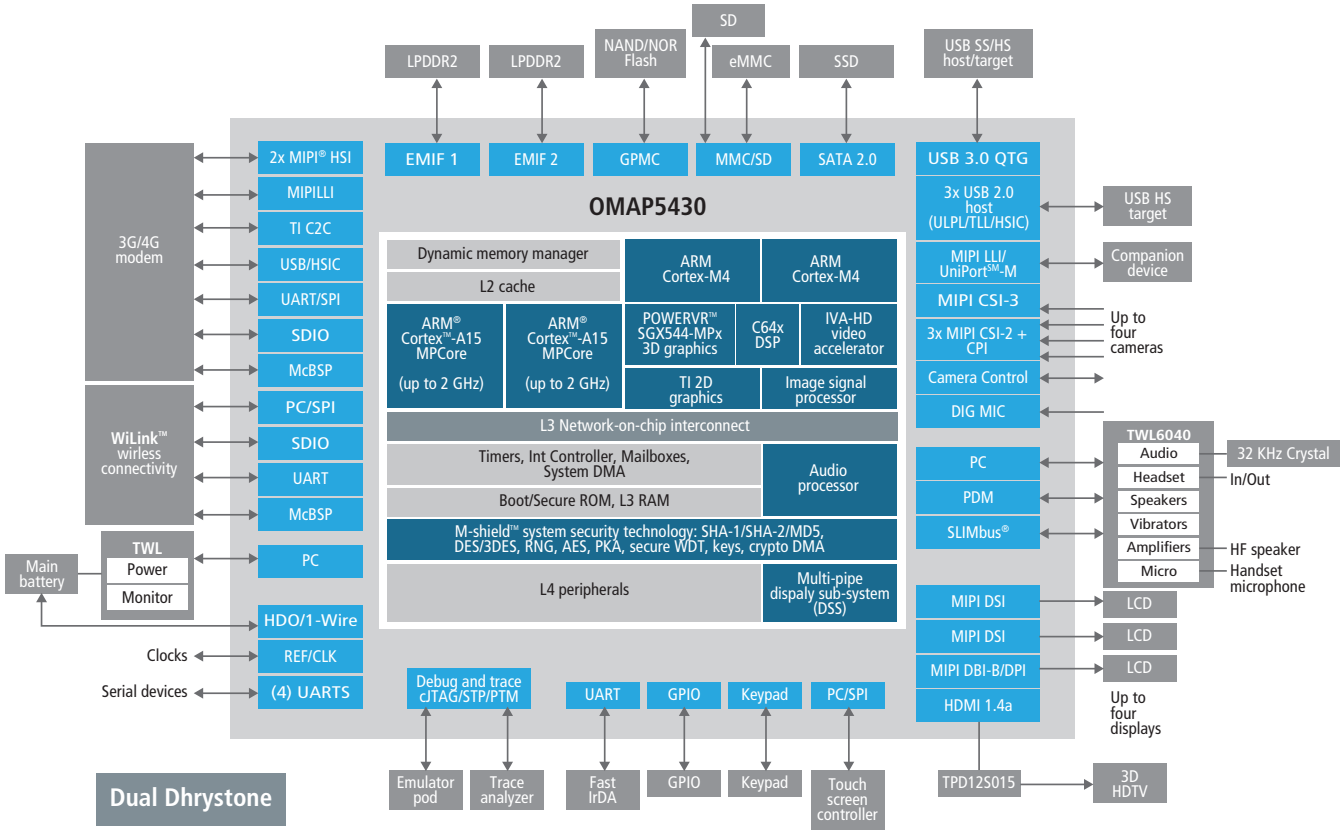
- Provide accurate power estimation based on real use cases
- Develop a methodology and a power dashboard, and continually track power updates
- Achieve close correlation between an architect's power estimation and actual silicon measurement

Cadence Solutions

- Palladium XP Dynamic Power Analysis
- Encounter Power System

Results

- Power estimation and actual silicon measurement at 96% accuracy
- Detected unexpected power peaks and resolved design to lower power consumption



The Challenge

For smartphone and tablet markets, as well as for most embedded markets, including automotive, both power consumption and performance are critical differentiators to TI customers.

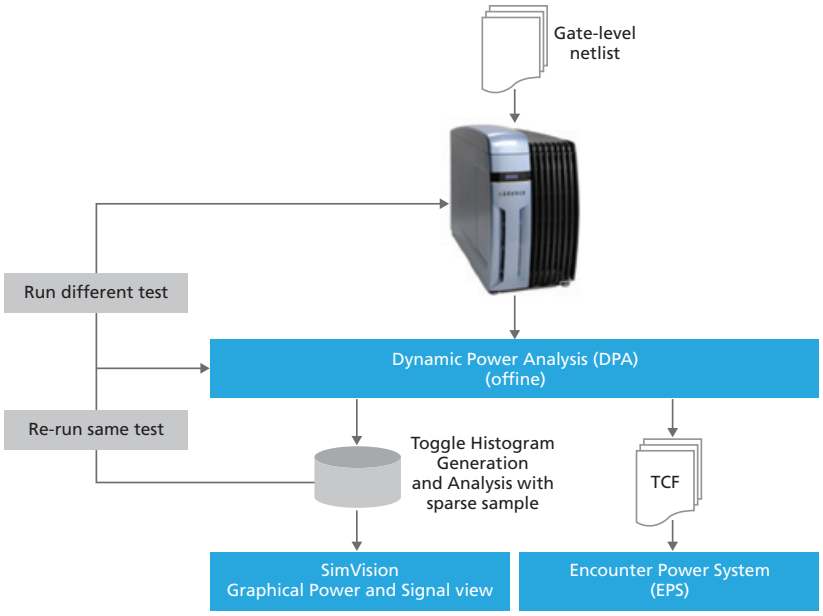
Application processors need higher performance to manage multiple applications, including phone calls, simple web or document browsing, playing and recording high-density videos, and playing 3D games. In addition, these processors have aggressive battery-life requirements, and it's important to estimate power consumption early in a project cycle to ensure that silicon reflects the original power estimation.

TI knows it's not just a matter of process technology business, where a technology shrink will decrease power consumption and increase performance. What's needed is aggressive power management, which requires estimating the power for all user actions performed in the final hardware system stimulated by software controls.

The traditional path of power estimation starts with a power architect's measurements from a previous project, supplemented with technology scaling, and then optimized based on design architecture. The architect also defines some typical use cases, with early estimates of the power for use case.

When verifying the integrated circuit design with an HDL simulator and a power tool, the different use-case scenarios are run and toggle-count information is extracted. The toggle count, along with a physical formula, yield an estimated power.

The challenges with estimating power using HDL simulation with a gate-level netlist are typically that the runtimes are extremely long and the time to generate a standard simulation output file can take several hours. In addition, the size of the output file can be several gigabytes for a very limited time window. Alternatively, vectorless power estimations using power tools yield pessimistic power results at best since they don't contain any toggle data. So correlations to the real power consumption of the silicon aren't realistic.



The Solution

Cadence® Palladium® XP Dynamic Power Analysis (DPA) significantly improved TI's flow and methodology. A gate-level netlist, generated from TI's back-end tools, was compiled into the Palladium XP hardware.

After the TI team completed a run in an accelerated environment, it post-processed the data using DPA in an offline session. This freed up the Palladium XP hardware for other verification and validation tasks.

TI was initially concerned about zero-gate-delay timing representation in the Palladium XP hardware, but the quality control (QC) tests passed at the first trial. TI compared the toggle information against a golden estimation from a Dhrystone use case, and after running the first dual Dhrystone use case on Palladium XP with the Cortex-A15 processor, TI exported the toggle count format (TCF) files and read into Cadence Encounter® Power System to add power rail information, giving better accuracy.

The results from the Palladium XP DPA were within 96% of TI's expected power consumption. In addition, by running longer runs in Palladium XP compared to simulation, TI was able to detect unexpected power conditions as the design was stimulated with actual software for real use-case scenarios. Once silicon was available, TI ran the same tests and after the normalizing step, it observed a greater-than 90% correlation between Palladium-Encounter Power System power estimation and silicon measurement on the clock trees.

Initial successful trials with Palladium XP DPA and Encounter Power System have opened up the door for much more complex use cases such as stress testing all memories interfaces, graphics processing unit (GPU) and HD video. TI has established a way to leverage the power flow and has discovered an ultimate design-validation experience.

Summary

With Palladium XP DPA, combined with Encounter Power System, TI achieved very close correlation between the architects' power estimation and actual silicon power consumption measurements, enabling the company to deliver the best thermal and power experience to its customers. TI applied real use cases to visualize the full power consumption, enabling engineers to focus on resolving unexpected power peaks.

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