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STMicroelectronics and Cadence

"The formal verification approach proved to be a complete answer to our STxP70 IP customers' integration challenges… and it was quite easy for us to customize for our specific case."

Jean-Paul Henriques, STxP70 Verification Team Leader, STMicroelectronics

The Customer

STMicroelectronics STxP70 processor technology offers a cost-effective, real-time optimized, 32-bit RISC system. It can be integrated into systems on chip (SoCs) in individual or multi-processor (MP) configurations. The flexible configurations and custom extensions allow the STxP70 to be efficient in many varied applications, but this creates another component to be integrated with the STxP70 core. Hence, STxP70 customers need to pay special attention to integrating the STxP70 into their designs, especially when it comes to verifying the connectivity between the core and extensions.

The Challenge

Before the formal verification flow was introduced, verification of the STxP70's correct integration into the customer's design was manual and error-prone. Verification of the connectivity was carried out by a combination of manual inspection and "directed test" simulation. Given the complexity of the interface, with point-to-point, point-to-multipoint, multiplexed, and ORed connections, it was possible to create mismatches and hard to detect them. This process led to extended verification times, typically 3 to 4 days of non-exhaustive checks, and potential late discovery of bugs, causing schedule impact and quality issues for the STxP70's customer projects. In one instance, what was thought to be a bug in the processor core was found to be a connectivity issue after one to two months of investigation. As STxP70 Verification Team Leader Jean-Paul Henriques explained, "Our customers' user experience with the STxP70 was not what we wanted it to be, and some of them complained about integration complexity. We knew we had to take a different approach."

Business Challenges

- Speed the time to market for developing SoCs incorporating STxP70 extensible processor

Design Challenges

- Simplify and accelerate the integration of STxP70 extensible processor and extensions into SoC-based designs

Cadence Solution

- Cadence Incisive Formal Verifier
- SoC Connectivity verification application (customized by STMicroelectronics for STxP70 core plus extensions)

Results

- Easy-to-use, high-performance solution, even for formal verification novices
- Exhaustive connectivity checks completed in 15-30 minutes, compared with 3-4 days for non-exhaustive checks previously
- Found connectivity issues 1-2 months earlier than previous methods

The Solution

Richard Le Roy, verification engineer on the STxP70 team, put together a custom verification application implementing the flow illustrated in Figure 1. After the STxP70 is compiled and elaborated, designers use a form-based GUI to capture the paths to the design files for the configured core and its extensions, each one essentially being an additional IP block.

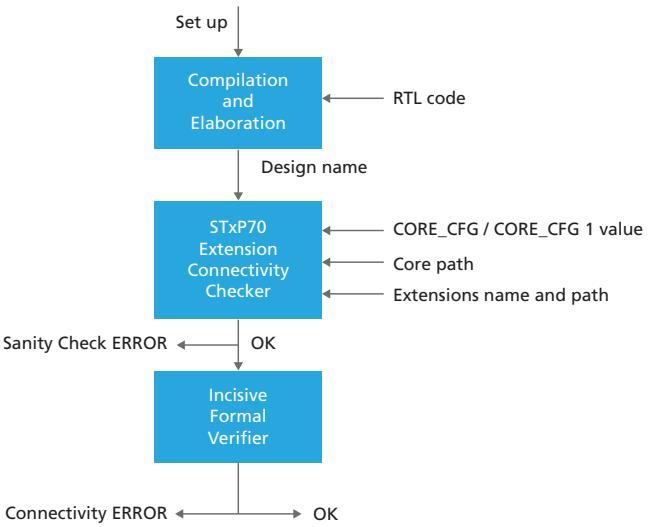

Figure 1: STxP70 Extensions Connectivity Checker Flow

The custom verification application creates the top-level connectivity and sanity-checks it. This step replaces manual editing of the spreadsheet in the previous flow. The connectivity checker automatically generates assertions in Tool Command Language (TCL), enabling exhaustive connectivity verification in the Cadence® Incisive® Formal Verifier tool. The application uses an Incisive Formal Verifier capability to automatically "black box" unnecessary logic, thus reducing runtime to attain a complete verification result.

The verification application's custom form-based GUI is shown in Figure 2. Figure 2 also shows the results of connectivity checking for an example variant of the STxP70, presented in the Cadence SimVision debugger, which is the results viewing and debug tool that is common across the complete Incisive family of verification products, including Incisive Formal Verifier.

Connectivity verification can be completed in approximately 15 minutes, typically, with 30 minutes the maximum runtime for more complex STxP70 implementations. "Connectivity verification is naturally handled most efficiently by a formal verification application, compared with simulation and test benches," said Le Roy.

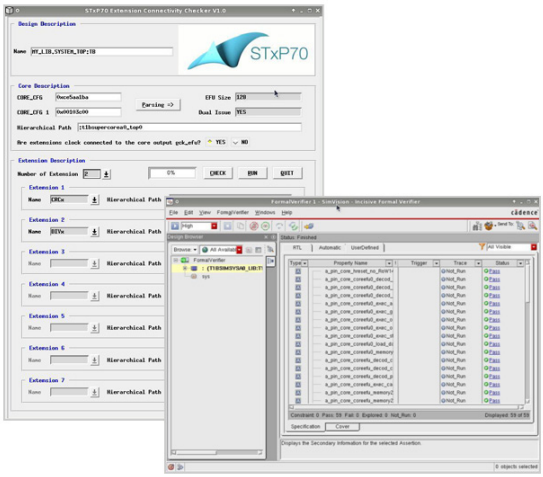

Figure 2: Connectivity Checker GUI and Results in SimVision Debugger

Results and Summary

The custom connectivity verification application proved to be easy to use, even for customers completely new to formal verification and STxP70. Connectivity verification could be completed in approximately 15 minutes, typically, with 30 minutes the maximum runtime experienced for more complex STxP70 implementations, compared with approximately three to four days to complete the previous non-exhaustive checks. The inter-connect capture and assertion generation parts were completely automated, requiring only STxP70 IP-specific information to be added by the customer. The verification application supports all connectivity types, including ORed connection support, necessary for STxP70. Henriques summarized that "the formal verification approach proved to be a complete answer to our STxP70 IP customers' integration challenges… and it was quite easy for us to customize for our specific case."

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