

STMicroelectronics and Cadence

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S. Sayar, Sr. Verification Engineer, STxP70 Team, STMicroelectronics

The Customer

STMicroelectronics is a world leader in providing semiconductor solutions for a wide range of application areas that make a positive impact on people’s lives, today and in the future. The company’s Unified Platform Division resides in Grenoble and part of this group is the STxP70 team. The STxP70 team is responsible for defining, developing, and verifying the configurable processor and peripherals that are used across multiple worldwide divisions within STMicroelectronics for many applications.

The Challenge

STMicroelectronics’s STxP70 team needed an efficient way to debug its register-transfer level (RTL) data cache IP flow, written in Verilog for design under test (DUT) and e language for testbench. The DUT and testbench environments are complex and configurable, leading to a significant knowledge ramp-up and important debug effort.

Unfortunately, the third party that created their testbench was no longer available to make any changes, and the team was not yet fully familiar with the environment. The team needed to quickly gain a deep understanding of the environment’s structure, variables, and sequences.

While performing RTL modifications, the team encountered many test failures. The team not only needed to quickly learn their testbench environment, they also needed an efficient and easy-to-use debugging tool.

Business Challenges

- Achieve faster debug of RTL data cache flow
- Quickly gain familiarity with new testbench for enhanced productivity

Design Challenges

- Learn testbench environment and manage debug process independently after support from testbench developer ended
- Detect and resolve bugs faster and earlier in the process

Cadence Solutions

- Incisive Debug Analyzer
- Incisive Specman Elite Testbench
- Incisive Enterprise Simulator
- SimVision

Results

- Saved 2 months of debugging time
- Enhanced team productivity with easy-to-use debug tool

The Solution

S. Sayar, Sr. Verification Engineer on the STxP70 team, was already familiar with Cadence® tools. He and his colleagues had been using Cadence Incisive® Specman Elite® Testbench for the past seven years for random test generation and to support fast, high-quality verification of its systems. Since the team was also using Cadence Incisive Enterprise Simulator as its Verilog simulator, it was most natural for him to suggest to his team Cadence Incisive Debug Analyzer.

“We were using print messages for debug, but using this method, we weren’t able to catch all of the errors and it was taking a really long time,” said Sayar. “Using Incisive Debug Analyzer, we were able to learn the structure of our third party-developed testbench environment step by step, and built a reliable environment for fixing bugs. Using Incisive Debug Analyzer, we saved two months in our overall debug cycle.”

“Previously, we had to keep re-running the simulation during our debug cycle, which wasted a significant amount of engineering time. Since Incisive Debug Analyzer provides an interactive debug flow in a post-process debug environment, our users have access to all the data files after the simulation. They only need to re-run the simulation once after the bug has been discovered -- a significant time saver in debug.”

Incisive Debug Analyzer provides comprehensive debug functionality in a single, integrated, and synchronized environment that supports multiple languages. Users have reported reductions in debug time by up to 50%. The tool helped the STMicroelectronics team find several kinds of bugs, thanks to the link and to the perfect synchronization between the Smart Log tab and the Playback tab window. Using these features, when a user has an idea that a failure could occur after or before the display of a particular message at a specific time, the user clicks on that message in the Smart Log tab window, then gets to the Playback tab to start debugging backward or forward by stepping in the code. The STMicroelectronics team was able to quickly debug all of its `dut_errors()`.

Among the tool tabs the team found to be the most useful:

- Playback Debugger, which enables users to either step or jump through time to any source code line or even to a variable change. With this feature, users can perform an interactive, step-by-step debug in post process – both forward and backward in time
- Smart Log window, an integrated message window that shows logfile messages from HDL, testbench, C/C++/SystemC/ assertions, and more

- Search, which provides efficient ways to filter log files or search for signals and variables used in the design
- Variable Value, which allows users to see all internal variable values at any point of the simulation, including those that cannot be dumped into the waveform database

Incisive Debug Analyzer explores the Specman Elite Testbench and the company’s RTL design environment. The team simply launches the Incisive Debug Analyzer GUI to access the information and start the debug process. Leveraging the metric-driven verification methodology, the team took advantage of a variety of checkers: protocol, data integrity, and performance, to name a few.

“I keep the GUI for Incisive Debug Analyzer on all day, because I’m using the tool often. In fact, every day, I discover a new feature of the tool that helps us during the debug process,” said Sayar.

The Benefits

In addition to saving two months on its debug cycle, the STMicroelectronics team also gained the confidence to guarantee the quality of its IP verification before integrating the RTL data cache IP into a system-on-a-chip (SoC) application. Incisive Debug Analyzer helped the team find and repair some functional defects in its IP and also quickly learn its testbench environment.

The team also enjoyed a close collaboration with Cadence on its verification flow and methodology. “We appreciate the availability and efficient support provided by Cadence,” noted Jean-Paul Henriques, manager of the STxP70 team. “In particular, the workshop events organized by Cadence every two to three months were very helpful in helping us understand the new technologies and methodology provided, as well as in enabling us to quickly learn how to fully utilize Incisive Debug Analyzer in our environment.”

Summary and Future Plans

Pleased with the results delivered by Incisive Debug Analyzer, STMicroelectronics’s STXP70 team is now using the tool to debug its direct memory access (DMA) IP. In addition, the team has provided Cadence with feedback that will help to continually enhance the tool.

“We enjoyed the teamwork with Cadence as we implemented Incisive Debug Analyzer into our environment,” said Henriques. “Based on the efficiency gain we’ve already seen with the tool, we can see ways to extend the benefits deeper into our company by using the tool in other flows worldwide.”



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