

SpeedBridge Adapter for PCIe 4.0

System emulation under real-world operating conditions

The Cadence® SpeedBridge® Adapter for PCI Express® (PCIe®) 4.0 provides efficient driver and application-level testing. Designed for pre-silicon RTL and integration of PCIe-based ASICs and systems on chip (SoCs), the solution can reproduce post-silicon bugs, as the design runs in the actual target system. The solution verifies emulated PCIe 4.0 designs with the actual ASIC/SoC software/ hardware, driver development, and application development, and runs with existing software and software test programs. Efficient and rapid adoption of the SpeedBridge Adapter for PCIe 4.0 is possible through the use of the Cadence Emulation Development Kit (EDK) platform that provides a pre-validated, off-the-shelf, datacenter-ready emulation server with the SpeedBridge adapter pre-installed.

Addressing Verification and Integration in PCIe Devices

PCIe is a high-bandwidth, low-pin-count serial interconnect technology that also maintains software compatibility with older PCI infrastructure. It's uniquely positioned as the logical interconnect technology for today's products.

With the SpeedBridge adapter, you can address the verification and integration needs for your PCIe devices. The solution consists of an interface card and emulator-resident Verilog wrapper that transparently convert a standard PCIe interface into an emulation-speed PCIe interface (see Figures 1 and 2). It performs rate adaptation so the emulated PCIe device can connect to a full-speed PCIe device. The plug-and-play card is compatible with standard PCs, workstations, and most embedded PCIe platforms without requiring modification. Similarly, an emulated root complex can connect to the full-speed endpoint cards through a standard PCIe backplane.

The SpeedBridge adapter connects directly to a Cadence Palladium® Z1 Enterprise Emulation Platform through

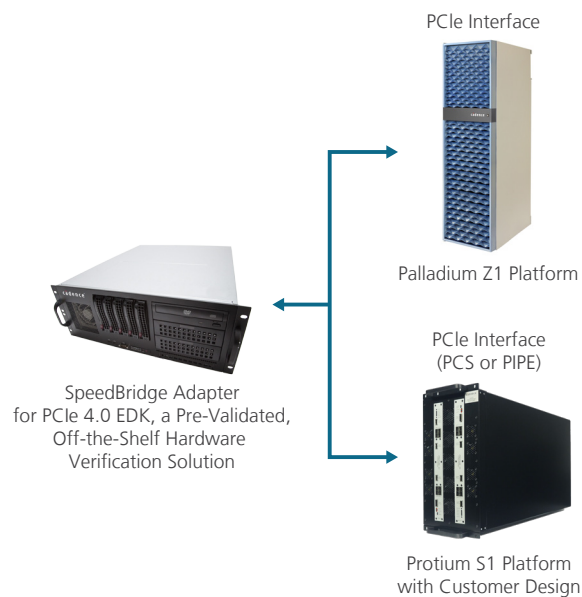


Figure 1: System components for endpoints emulation

standard emulation cables and adaptors. The SpeedBridge adapter is also compatible with the Cadence Protium™ S1 FPGA-Based Prototyping Platform through a Protium S1 interface card. It is designed to be functionally transparent to both the PCIe 4.0 host or device. As a result, most software applications and device

drivers developed for the device under test (DUT) can be used without modification in the PCIe test environment. Because of the high speed of in-circuit emulation and FPGA-based prototyping, a user can co-verify hardware and software together with software drivers before silicon is available.

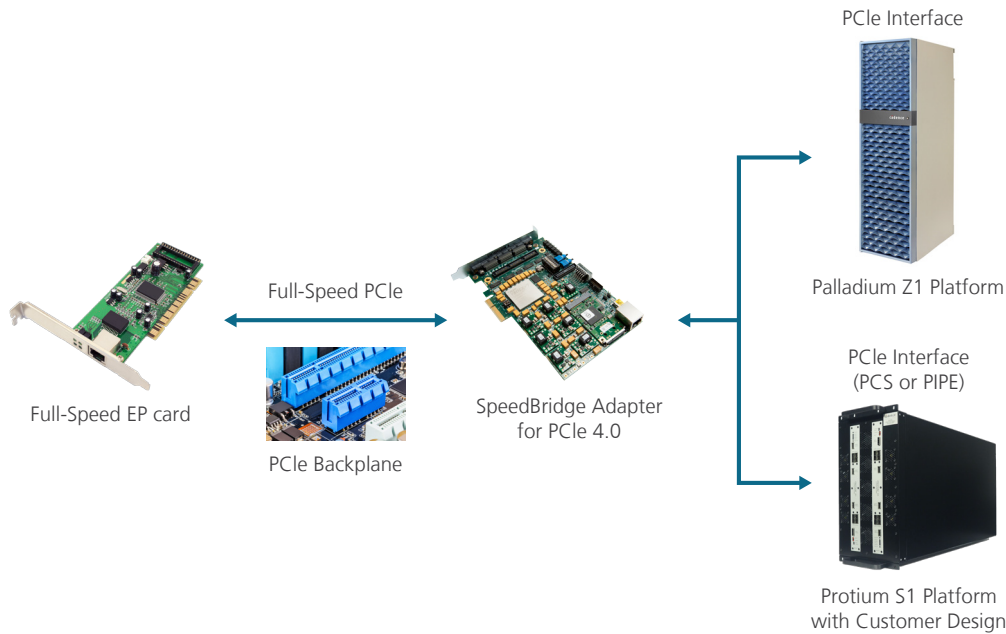


Figure 2: System components for root complex

Traditionally, software debug with an RTL Logic Simulator is not practical because it consumes billions of simulation cycles. In addition, there is also software (e.g., device drivers) that requires a physical system that cannot be easily connected to a simulator. Cadence emulators and FPGA-based prototyping systems provide the advanced hardware/software debug capabilities needed for ease of use, ease of debug, and high speed—without sacrificing quality. The solution also supports quick system bring-up, getting application-based traffic running in a short span of time.

Benefits

- Enables rapid emulation and prototyping deployment
- Enables verification IP reuse
 - Works from one project to another
 - No need for every user to create custom solutions
 - Improves productivity to get to the first test by leveraging existing applications, third-party software tools, and more
 - Eliminates the need to set up a complex custom-built environment
- Ensures quality
 - Technology tested and verified by Cadence and many other user designs

- Verifies designs quickly and efficiently
- Provides a single-card solution
- Reduces system risk
 - Checks PCIe protocol and integrity errors (e.g., CRC)
 - Runs real system software/drivers
 - Verifies the PCIe design in real environments, allowing both hardware and software interoperability
 - Allows for testing of different OSs, different chipsets, and other real PCIe hardware platforms
 - Increases confidence in PCIe device quality
 - Reduces time to market

Hardware Features

- Compliant with PCIe Base Specification V4.0
- Enables emulation of root complex, endpoint, switch, and bridge devices
- Compatible with non-SSC/SSC (Spread Spectrum Clock) PCIe 4.0 platforms
- Supports link-speed negotiation of 2.5Gbps, 5.0Gbps, 8.0Gbps, or 16.0Gbps with the emulated PCIe 4.0-capable designs
- Supports SR-IOV
- Supports power management states:
 - L0—Normal mode
 - L0s—Link suspended

- L1 and L1 sub-states with CLKREQ#—low-power state
- Multiple lanes
 - Support for 1x, 2x, 4x, 8x, and 16x lanes
- Works with emulation speeds of up to 2MHz
- Backward compatible with PCIe 3.0-, 2.0-, 1.1-, and 1.0a-based designs
- Connects an emulated PCIe 4.0 device to a full-speed (2.5Gbps/5.0Gbps) PCIe interface

Software Features

- Functionally transparent to most software driver or operating systems
- PCIe driver environment
 - Installs in PCIe host platforms when emulating an endpoint device
 - The driver runs in the emulation system in the Palladium Z1 or Protium S1 environment when the DUT is root complex and it needs to talk to external end-point devices
- Enables early debug with first silicon and first software
 - Concurrent software development and hardware/software co-verification
- Debug capabilities

- SpeedBridge Adapter for PCIe 4.0 is a fully static implementation allowing support for key emulation debug features when used with Cadence EDK
- Support for industry-standard protocol analyzers
- Emulation protocol monitors provided
- Includes SpeedBridge Configuration Manager software, which runs on your workstation to remotely monitor the PCIe interface status

Specifications

The SpeedBridge Adapter for PCIe 4.0 supports:

- Memory, I/O, configuration, and message transactions
- Requests and completions
- Complete PHY-level link initialization including TX equalization
- System-driven, credit-based flow control
- PCIe PHY-level 10-bit and 20-bit interfaces as well as standard PIPE in either 8-bit, 16-bit, or 32-bit mode
- One virtual channel (VC) and one traffic class (TC)
- Payloads from 128-byte to 4096-byte
- Legacy and non-legacy devices
- Supports PCIe 3.0 and 4.0 PIPE3/PIPE4 equalization interface
- Lane reversal and polarity inversion
- Extended configuration space
- Transaction ordering driven by host platform
- Multiple read completion
- For detailed information, email cva_support@cadence.com.

Requirements

- One SpeedBridge Adapter for PCIe 4.0 for each emulated PCIe interface
- A PC or workstation with two or more PCIe slots—two slots for each SpeedBridge adapter solution used for emulation endpoint devices
 - Second slot is needed for routing second cable out of the workstation
- A PCIe backplane for emulation of root complex devices
- System using Cadence Xcelium®, Protium S1, and Palladium series platforms
- Device drivers and/or application software required by the emulated ASIC/SoC
- Emulator-resident Verilog wrapper for SpeedBridge adapter for PCIe 4.0
- One Ethernet CAT5 cable for connecting SCM
- Requires two TPODS/HDDC

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training



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