DATASHEET

SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices

System emulation under real-world operating conditions

The Cadence® SpeedBridge® Adapters provide protocol interface solutions for an emulation platform that enables the efficient driver and application-level testing, targeting validation of pre-silicon RTL of ASICs and systems on chip (SoCs) with a Cadence Palladium® emulation system or Cadence Protium™ prototyping system. SpeedBridge Adapters can also be leveraged to quickly and easily reproduce post-silicon bugs. The solution enables verification of emulated designs along with development, testing, and performance characterization of embedded software, system-level drivers, and final software applications. The efficient and rapid adoption of the SpeedBridge Adapter is possible using the Cadence Emulation Development Kit (EDK) platform that provides a pre-validated, off-the-shelf, and data center-ready emulation server with the SpeedBridge Adapter pre-installed.

Pre-Validated, Off-the-Shelf Hardware Verification Solution

USB has become the world standard in connecting peripherals and mobile devices to PCs. An off-the-shelf emulation solution for USB designs, the SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices offers fast bring-up times, a fast path to a sophisticated verification platform, and an easy connection to a modern desktop and server-class PC systems running a variety of standard operating systems (OSs).

The SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices uses an industry-standard Extensible Host Controller Interface core (xHCI) found in modern desktop PC and server systems. The xHCI runs at emulation frequencies and communicates with the desktop PC across a standard PCI Express® (PCIe®)

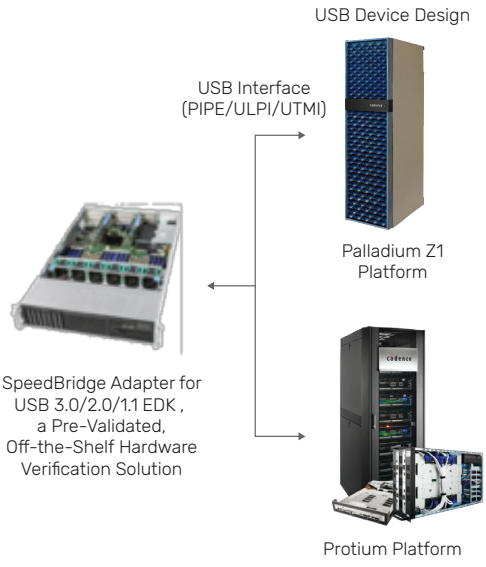

Figure 1: The SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices

bus. The SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices enumerates as a standard USB 3.2/2.0/1.1 xHCI host controller to the operating system and, therefore, does not require custom drivers. The USB 3.2/2.0/1.1 device under verification can be connected to the xHCI controller in the SpeedBridge Adapter and will be enumerated by the system OS through the SpeedBridge Adapter. USB device drivers can be installed on the system and the system OS will then have full access to the USB device using standard software APIs and across the standard USB PIPE, ULPI, or UTMI interfaces.

Using a standard digital interface that would normally connect to a USB PHY transceiver, the SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices can be connected to the device under test compiled for the Palladium series system verification computing platform. The SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices provides the necessary virtualization of the USB transceivers so that a USB device design mapped into a Palladium or Protium S1 platform will connect and configure in a normal manner as if a real transceiver were being used. It connects directly to either system through standard emulation cables.

The SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices transparently buffers the speed difference between the design mapped into the Palladium or Protium platform and the PC system, which means that both the design and the PC system are unaware of the speed differences and can use standard USB protocols to communicate.

With the extremely high speed of emulation and hardware prototyping available through the Palladium and Protium series platforms, the USB design can be co-verified in an environment that includes the USB device hardware design, the embedded device firmware, the low-level device driver, and the device application software running on top of the standard OS USB host software stack (see Figure 1).

The USB system environment includes a complex interaction of different layers of software and hardware, and the SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices allows debug and verification at many different nodes in the environment. For example, the inclusion of the entire USB software stack in the environment means that software engineers can install kernel-level OS software debuggers, along with third-party software packet analysis software to debug issues in the device drivers. The application software engineers can run standard software debuggers to debug their application software. Firmware engineers can run low-level GDB debuggers on the firmware running in the mapped design in the Palladium and Protium series systems.

In addition to the extensive software debugging that is enabled by the SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices, Cadence also provides tools to capture hardware-level PIPE streams of data that can be loaded into industry-standard third-party protocol analyzer software. This allows detailed protocol analysis of huge streams of packets flowing upstream and downstream between the Palladium series platforms and the PC system. Once issues have been identified in the large, complex streams of data, it is then straightforward to use the extensive, full-vision design debug capabilities of the Palladium series system. Or to move to higher levels of performance and throughput with the Protium series system.

Benefits

High-performance verification

- Offers the highest verification performance over all other methods without abstracting out critical portions of a real system
- Offers high-end verification performance that does not scale down the verification performance when used with multiple ports or multiple interconnect technologies
- Provides the fastest overall system-level verification performance when running a complete top-to-bottom real system environment

Rapid verification deployment

- Provides a pre-validated emulation interface fully compatible with the Palladium and Protium series platforms
- Enables the rapid creation of system-level environments using the same hardware and software that the real silicon will use
- Rack-mountable USB 3.2 EDK system can be deployed in data centers as a virtual resource connected to the verification platform
- Provides a dynamically relocatable resource that is accessible by remote users when used with the Palladium platform
- Allows quick and efficient design verification
- Provides a single card solution in a qualified server-class EDK system

Verification IP reuse

- Allows reuse between projects due to standards-compliant interfaces
- Eliminates re-implementation of custom per project verification environments
- Improves productivity by getting the design running quickly without weeks or months of specialized test environment creation: the PC system is the test environment
- Allows the use of standard third-party protocol analysis software

Ensured quality

- Tested and verified by Cadence against independent verification IP and other user designs
- xHCI core built on top of mature SpeedBridge technology has been deployed in many emulation environments over many years

Debug capabilities

- Supports key emulation debug features when used with Cadence EDK
- Support for logic analyzer debug capabilities

Reduced system risk

- Performs PIPE, ULPI, or UTMI interface testing at the physical level
- Runs full system enumeration connected to a real PC chipset running a real OS with a full USB software stack
- Does not abstract away low-level system connection issues that arise with real chipsets
- Does not abstract away the real enumeration sequence of different operating systems
- Runs the entire system-level suite, just as the design silicon will have to do when it is deployed, providing a necessary part of modern system verification
- Allows interaction with multiple system-level interconnects such as PCIe and Ethernet, all in the same verification environment and without impacting performance

Features

- Supports standard SuperSpeed 3.2 Gen 1 PIPE as described in “PHY Interface for PCIe and USB 3.0 Architectures Version 3.0”
- Supports standard UTMI+ level-2 interface to peripherals (no OTG)
- Supports standard ULPI interface to peripherals
- Supports PIPE 32-bit/16-bit interfaces
- Supports ULPI/UTMI 8-bit/16-bit unidirectional/bidirectional interfaces
- Supports HSIC interface
- Connects to verification systems using QSS cables to HDDC or TPOD
- PIPE/UTMI/ULPI interfaces are presented to the compiled design to look like a standard USB 3.2/2.0/1.1 PHY
- Models a virtual back-to-back PHY connection to the host controller in the SpeedBridge Adapter for USB 3.2/2.0/1.1 Devices
- Host controller uses a standard xHCI USB 3.2 Gen 1 register set, as viewed from the host system
- Supports Windows, Linux RHEL, Ubuntu, and other OSs with standard USB xHCI driver support
- Supports CONTROL, BULK, and INTERRUPT endpoint transactions
- Supports standard USB 3.2 Gen 1 transaction packets (TP), data packets (DP), and link management packets (LMP)
- Supports standard USB 3.2 Gen 1 LTSSM link training
- Supports USB 2.0/1.1 link and standard power modes including SUSPEND/RESUME signaling

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or internet. They can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24×7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.

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13625 03/20 SA/RA/PDF