cadence®

Renesas Deploys Cadence Interconnect Workbench with Palladium Z1 Platform

Renesas and Cadence

October 2017

Key Challenges

Each new generation of the Renesas micro controller unit (MCU) grows in complexity with more IP blocks, resulting in more complex and interconnected subsystems. As this complexity increases, more sophisticated interconnect performance validation efforts are required to verify that these IP blocks and subsystems function at the peak level of the system performance that is required of them.

Renesas continuously improves their methodology for developing performance verification environments and analyzing the results. With their previous approach, they analyzed performance at the IP and subsystem levels first, and then started their chip design cycle. As a result, finding performance issues, and validating that performance requirements are met, became more time consuming in the design cycle.

Renesas used to spend many days manually developing performance and functional verification environments and analyzing the results. They had been looking for a quicker and simpler way to verify their interconnects as well as measure and analyze performance data to achieve optimal system performance. As time-to-market requirements either stayed the same or shrank with each design cycle, this lengthy, and sometimes iterative, process became a bottleneck to faster design cycles.

Each new generation of MCU came with increased performance requirements, making throughput and latency of the interconnect crucial for success. And it quickly became obvious that these analyses needed to be done earlier in the design cycle to allow for changes in the design architecture.

"As design complexity increases with more and more IP integrated on a single chip, accurate performance analysis of off-chip memory access and on-chip interconnect becomes more crucial," said Toshinori Inoshita, senior manager, Shared R&D Division 2, Broad-based Solution Business Unit, Renesas Electronics Corporation.

Key Challenges

- Manually creating testbenches took days to complete
- Performance analysis typically required 22 days
- Performance simulations as long as 50 hours each

Cadence Solutions

- Palladium Z1 Enterprise Emulation Platform
- vManager Metric-Driven Signoff Platform
- Interconnect Workbench
- Incisive Enterprise Simulator

Results

- Reduced performance analysis from 22 to 9 days
- Improved verification execution speed by 250x

The Solution

Renesas adopted the Cadence® Interconnect Workbench in their design flow, along with the Cadence vManager™ Metric-Driven Signoff Platform and the Cadence Palladium® Z1 Enterprise Emulation Platform to solve this problem.

Renesas realized tremendous acceleration in their application-level performance verification by using the Palladium Z1 platform for their hardware acceleration flow, while executing production software use cases. The Palladium Z1 platform's very high performance enabled Renesas to conduct performance analysis of realistic scenarios of system performance. This allowed them to design for system-performance issues that arise out of complex real-world scenarios that normally would never have been seen during simulation, obscured by the complicated interactions that cause these scenarios.

Understanding system-level performance in complex MCUs with so many IP and peripheral interconnect blocks is a daunting task. Performance must to be analyzed and fine-tuned, not only at the individual IP block levels, but also at the overall system level to meet ever-increasing performance requirements. This involves cycle-accurate measurement that has traditionally been impossible until late in the design cycle, and typically performance problems are detected too late in the design cycle to make any high-level architectural changes to address them.

> *"As design complexity increases with more and more IP integrated on a single chip, accurate performance analysis of off-chip memory access and on-chip interconnect becomes more crucial"*
>
> Toshinori Inoshita, senior manager,
> Shared R&D Division 2, Broad-based Solution Business Unit,
> Renesas Electronics Corporation

By far, the biggest advantage that Renesas observed with the phased adoption of the Interconnect Workbench was that it enabled the performance verification at three different levels. Renesas used the Interconnect Workbench to:

- Characterize the latency of the MCU interconnect and bandwidth-critical paths, to measure their ability to meet the performance requirements of the IC
- Apply defined traffic loads on particular individual connections, and combinations of master connections, of the MUC interconnect, to test the performance and failure behavior under load
- Measure performance of traffic inside the MCU, including all the IP and software creating that traffic

These levels of verification allowed them to identify and address performance challenges very early on in the design cycle, and also address complex real-world scenarios later, so they could achieve their performance goals with minimal iteration, and greatly reduce their time to market.

Renesas also used the Interconnect Workbench to automate their latest generation of testbenches. This involved a single-step process to convert the input metadata that was in a CSV file, directly to Universal Verification Methodology (UVM) performance analysis and functional verification testbenches. The Interconnect Workbench also generated a testsuite to facilitate performance analysis, as well as functional verification. The intuitive and easy-to-use GUI, which enabled the designers to easily analyze and digest the performance metrics that they were seeing in their design, allowed for early detection of performance bottlenecks and early validation of system performance requirements.

The Results

The Interconnect Workbench, used in conjunction with the Cadence Incisive® Enterprise Simulator and vManager Metric-Driven Signoff Platform, enabled early detection of performance issues and early validation of system performance requirements on an integrated environment. Renesas also used the Interconnect Workbench together with the Palladium Z1 platform to accelerate the application-level performance analysis and verification while emulating software loads on their design and reducing 50-hour simulations to a typical 12 minutes of emulation time, a 250x improvement. These results were initially presented at CDNLive Japan in 2016.

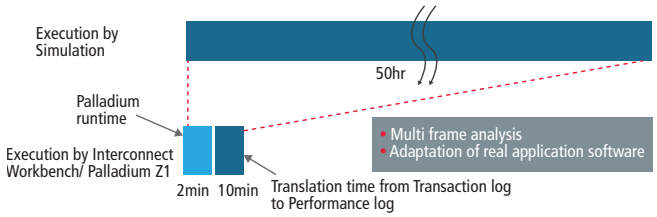

Figure 1: Time savings from Palladium runtime and Interconnect Workbench post-processing

The Interconnect Workbench automation reduced performance analysis time from a typical 22 days to an average of 9 days. This automation included automatic generation of testbenches and testsuites, and an easy to use GUI for display of results and interactive performance debugging.

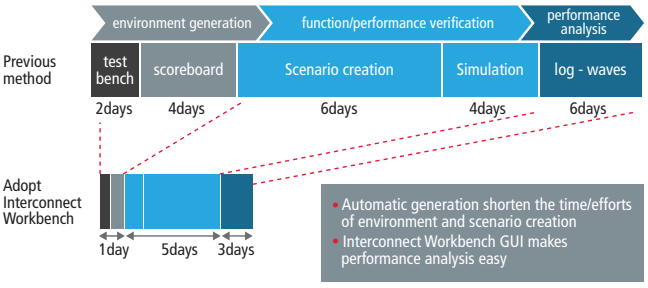

Figure 2: Time savings using Interconnect Workbench versus manual approach

In addition, the use of Palladium enabled the team to bring up the entire design and run firmware and real use case tests. This enabled Renesas to design for complex real-world traffic, meeting their performance goals faster, and with greater confidence.

Summary

Renesas used the Interconnect Workbench to accelerate performance analysis and verification of their on-chip interconnects, reducing performance analysis from 22 days to a typical 9 days. The Interconnect Workbench provided Renesas with a cycle-accurate performance analysis of interconnect throughout the MCU design process by quickly identifying bottlenecks under critical traffic conditions, enabling Renesas to improve device performance and reduce time to market.

"The Cadence Interconnect Workbench is a unique tool that allowed us to accurately monitor the performance of on-chip interconnect, dramatically improving the turnaround time for design architecture exploration," said Mr. Inoshita, while discussing the company's future plans with Cadence. "We're planning to adopt this technology on additional new design projects at Renesas."

cadence®

Cadence software, hardware and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. The company's System Design Enablement strategy helps customers develop differentiated products—from chips to boards to systems. **www.cadence.com**