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Building a State-of-the-Art Verification Environment

Renesas and Cadence

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The Customer

A global leader in microcontroller (MCU), analog, power, and system-on-chip (SoC) products, Renesas Electronics Corporation is a Japanese semiconductor manufacturer headquartered in Tokyo. It has manufacturing, design, and sales operations in approximately 20 countries. Renesas' market-proven MCU and SoC products and technologies offer an exciting and diverse range of opportunities throughout key market segments such as automotive, industrial, cloud computing, healthcare, and the internet of things (IoT).

The Challenge

The challenge faced by Renesas was that they were developing a new data conversion block, including an AHB bus bridge, which would be added to an existing DMA IP core. This new module also had a complicated finite state machine (FSM).

They needed a short turnaround time with a limited number of engineers, while maintaining Renesas' high-quality standards for IP core development. To that end, they wanted to reuse some in-house IP cores and their verification in the new design project, using a new team not familiar with the previous projects.

In addition, Renesas was aiming to refresh their verification methodologies with the most cutting-edge technologies. The verification environment of this project should be a model case to improve the productivity of succeeding IP core design projects.

Renesas turned to Cadence for help.

The Solutions

Using Cadence® tools and leveraging the help from Cadence Japan application engineers (AEs), Renesas figured out how to make the tools work together to verify this complicated data conversion block.

Specman Elite with Xcelium Parallel Logic Simulator

Renesas had used a legacy simulator and debug tool with Cadence Specman® Elite in the original project. The original use of Specman Elite resulted in a testbench written so well that the verification engineers could use the ***e*** language's native scalability. This was successful, despite the fact that there were over 45 component files, and many internal connections spanned across components.

Key Challenges

Build an environment with state-of-the-art verification technologies, as a model case for succeeding projects, with:

- Maximum reuse of legacy IP cores and verification environments
- Short turnaround time
- High-quality results

Cadence Solutions

- Specman Elite + Xcelium Parallel Logic Simulator with Indago Debug Analyzer App
- JasperGold Formal Verification Platform and Apps
- vManager Metric-Driven Signoff Platform

Results

- Overall 77% decrease in projected labor costs
- High-quality results
- Renewed verification environment with cutting-edge Cadence products

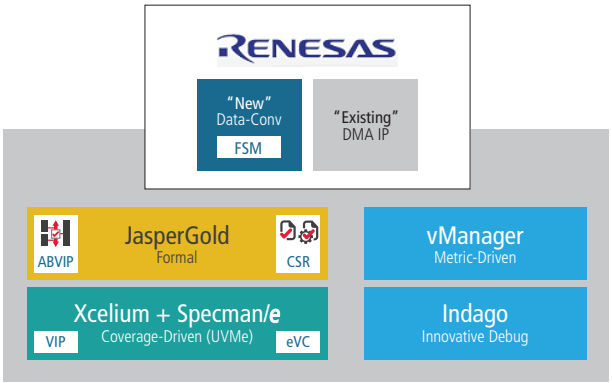

Figure 1: Renesas Verification IP environment with Cadence verification solutions

The verification IP (VIP) provided already-proven AHB protocol generation and analyzing features, so the engineers could omit development time of the AHB models. After bringing up the testbench, the Renesas engineers could enjoy the native extensibility of the ***e*** language and Specman Elite.

Renesas then introduced the Cadence Xcelium™ Parallel Logic Simulator alongside the Cadence Indago™ Debug Analyzer App, leveraging the aspect-oriented programming (AOP) capabilities of the ***e*** language for constructing sophisticated and scalable testbenches.

Indago Debug Analyzer App

Indago Debug Analyzer App helped Renesas engineers rapidly apply the existing Specman environment for the new design and helped the new team quickly understand and become effective with the reused verification content. The feature that synchronously displays simulation-waveforms and corresponding AOP-class elements enabled the engineers to reveal the many internal connections across the 45 component files. Because the Indago Debug Analyzer App stored all necessary data during a single simulation execution, a significant amount of development time of the testbench could be saved by avoiding simulation iteration, which had been required by conventional debug tools.

Some of verification processes were shortened from one day to a few hours, because of reduced simulation iterations and the intuitive data exploration feature of the Indago app. The verification team succeeded in an 82% reduction of labor costs.

JasperGold Formal Verification Platform and Apps

The Renesas verification team adopted the Cadence JasperGold® Formal Verification Platform, including the JasperGold Formal Property Verification (FPV) App with Scoreboard, JasperGold Control and Status Register (CSR) Verification App, and the JasperGold Superlint App. The FPV app, the Scoreboard feature, and Cadence Assertion-Based VIP allowed Renesas to start the verification effort before finishing the simulation testbench bring-up. "What if?" analysis capabilities with the JasperGold Visualize™ Interactive Debug Environment and the Jasper QuietTrace™ debugging capability made early-stage bug hunting easier. The JasperGold Superlint App played an important role in FSM deadlock analysis.

> *"To make the best use of the existing IP cores, renewing the legacy verification environment with the most advanced tools available proved to be an effective approach. Positive and collaborative relationships with Cadence played a key role to achieve it."*
>
> Takahiro Ikenobe, Director, Peripheral Circuit Design Department, Shared R&D Division 2, Broad-Based Solution Business Unit, Renesas Electronics

The JasperGold Apps and Assertion-Based VIP found 64% of the bugs revealed during this phase of verification, with 36% found by simulation. The result was that the new FSM verification labor effort were reduced by 56%, all while achieving a high quality of verification by evaluating test cases in the early phase.

vManager Metric-Driven Signoff Platform

The vManager™ Metric-Driven Signoff Platform's combined coverage helped Renesas to ensure that both dynamic verification and formal verification efforts fully contributed to verification signoff. Their combined coverage reached 100%. Renesas engineers and Cadence application engineers worked together on constructing an automation environment with the vManager platform so succeeding IP projects would be able to use it for automating from the simulation and formal executions through their aggregated analysis.

Summary Results

Overall, using Cadence products resulted in an overall savings of 77% in labor effort, all while satisfying Renesas' demand for high quality. Most of the reduction in labor is attributed to the combination of the Specman Elite, Xcelium Parallel Logic Simulator and Indago Debug Analyzer App. Combined coverage in the vManager platform reached 100%, allowing Renesas to confidently achieve verification signoff.

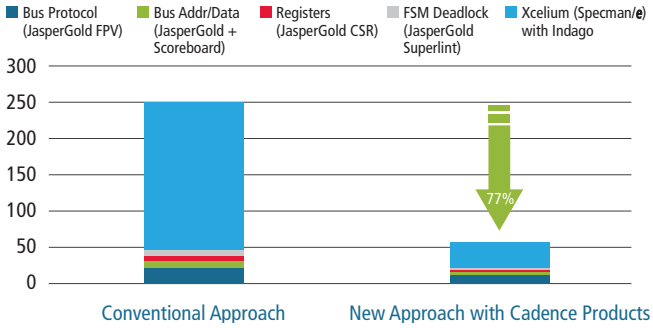

Figure 2: Labor days cost comparison

By renewing their verification environment with Cadence's cutting-edge EDA tools, the Renesas project team succeeded in maximizing the reuse of their legacy IP core and meeting the target schedule. This approach was a great step forward for making the most of in-house IP.

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