

QLogic and Cadence

“Palladium XP is an essential tool that enables us to successfully develop our ASICs and to verify our design much earlier in the production cycle. This equates to cost, time, and money savings while helping us bring products to market much faster.”

Greg Kleese, Vice President, Network Solutions Group, QLogic

The Customer

QLogic is a leader in converged networking, enterprise Ethernet, and storage area networking (SAN) products. Using a flex-port architecture in its application-specific integrated circuits (ASICs), QLogic provides end-to-end, integrated solutions that address the broad networking spectrum.

QLogic manufactures Fibre Channel and Ethernet converged networking solutions for successful integration into data centers. These switches provide the port-density and performance required to drive storage and data networks of leading original equipment manufacturers (OEMs) and end users worldwide.

The Challenge

To continue to expand its market share, QLogic must consistently deliver technologies that transform data centers and storage networks around the globe. “Specialized systems on chip (SoCs) enable us to deliver network switches optimized for our customers’ power, performance, and bandwidth requirements,” explains Greg Kleese, Vice President, Network Solutions Group, QLogic.

With this goal in mind, QLogic needed to speed the design and verification of a complex new network switch. This multi-million-gate SoC was needed to drive scalable, non-blocking switch architectures across the various protocols required from data center-class switching solutions.

“In this type of design and verification, we have large numbers of ports in the switch design,” explains Tom Paulson, Verification Engineer for the Network Solutions Group, QLogic. “Being able to test all the ports at one time is critical. We’re also being asked to simulate the design at the system level much sooner in the design cycle.”

Business Challenges

- Quickly produce a sophisticated new network switch to capture market share

Design Challenges

- Ensure success of complex ASIC design with system-level verification

Cadence Solutions

- Palladium XP Verification Computing Platform
- Customer Support

Results

- Achieved verification of an ASIC design at the system level, earlier in the design cycle and faster than in previous ASIC verification projects
- Reduced verification time by 50% compared to previous, less-complex switches

The Solution

To meet its stringent time-to-market requirements for the network switch, QLogic turned to the Cadence® Palladium® XP Verification Computing Platform. Using Palladium XP, the company was able to dramatically reduce the design and verification time.

“The Palladium XP platform enabled us to verify our design at the system level much earlier in the design cycle and much faster than ever before,” Paulson says. “We’re very happy with the platform’s performance and capacity.”

Previously QLogic used Palladium II, but decided to upgrade to XP due to the size and complexity of the new design, and the need to simulate the full ASIC before tapeout. “Before buying Palladium II several years ago, we considered other vendor solutions,” Kleese says. “But since we’ve had so much success with Palladium II over the years, it was an easy decision to move to Palladium XP”

The QLogic design team found it was very easy to ramp up from Palladium II to Palladium XP. There was very little learning curve and the migration was fast.

“The Palladium XP platform enabled us to verify our design at the system level much earlier in the design cycle and much faster than ever before.”

“Once we decided to upgrade, we started changing scripts and testbenches,” explains Mark Neutz, Verification Engineer for the Network Solutions Group, QLogic. “By the time we received Palladium XP, it was only a couple of days before the platform was up-and-running on production jobs.”

Palladium XP supports design configurations up to 2 billion gates, delivering performance up to 4MHz and simultaneously supporting up to 512 users. The platform unifies simulation, acceleration, and emulation capabilities in a single environment, enabling efficient hardware/software system co-verification.

“With Palladium XP, our design teams can ‘hot swap’ simulation with acceleration and emulation in a scalable, metric-driven verification environment,” Kleese says. “This speeds our verification process and enables us to start testing embedded software and evaluating performance much more quickly.”

QLogic used the platform to simultaneously explore the complex interaction of buses, ports, and crossbars at the system level. The company leveraged the capacity, speed, and debugging capabilities of Palladium XP to reduce the verification time associated with its latest ASIC design, even compared to earlier, less-complex ASICs.

“With its much deeper trace buffer, Palladium XP enabled us to examine a trace window more than 10 times the size of previous-generation switches,” Neutz says. “This is a requirement for system-level verification of high node-count switch designs.”

Palladium XP also provided the capacity required for QLogic to create a synthesizable testbench. The company was able to incorporate testbench parameters into read-only memory (ROM) for advanced system-level testing. The highly scalable system easily accommodated the QLogic multi-million-gate design, while giving the company room to grow for next-generation designs.

Another key benefit of the Cadence solution, according to Neutz, is dependable customer support. “When we initially looked at Palladium XP, we had a lot of help from Cadence Customer Support,” he says. “That really made our jobs easier, because we don’t have time for things not to work. The transition from Palladium II to XP was fast, painless, and problem-free, thanks to the great support staff.”

Summary

The capacity, speed, and debugging capabilities of Palladium XP enabled QLogic to dramatically reduce the design and verification time on its complex new network switch.

“We’re being asked to do more with system verification than ever before, in shorter timeframes than ever before,” Kleese concludes. “Palladium XP is an essential tool for successful development of our ASICs. I don’t see how we could meet our design goals and continue to grow our market share without it.”



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com