

Protium X1 Enterprise Prototyping Platform

Early software development and high-performance system validation

Your designs are getting bigger and your embedded software is growing exponentially. Yet, your development schedules are shrinking, and you must complete your projects earlier. Consequently, new tools are needed to address these ever-growing challenges.

The Cadence® Protium™ X1 Enterprise Prototyping Platform is a first-of-its-kind enterprise prototyping platform. Architected from the ground up to provide extreme scalability and flexibility in a datacenter-optimized form factor, it is addressing your requirements of today, and growing with you, as your designs and demands are growing tomorrow.

The Protium X1 platform combines a modern, blade-based hardware with the industry-leading implementation and debug software suite that ensures that your FPGA-based prototype comes up quickly, reliably, and has everything you need to start firmware and software development early. The Protium X1 platform is the platform of choice for early firmware/software development, high-performance hardware regression, and full-system validation.

The Protium X1 platform is part of the Cadence Verification Suite, which consists of best-in-class core engines, verification fabric technologies, and solutions that increase design quality and throughput, thus fulfilling verification requirements for a wide variety of applications and vertical segments.

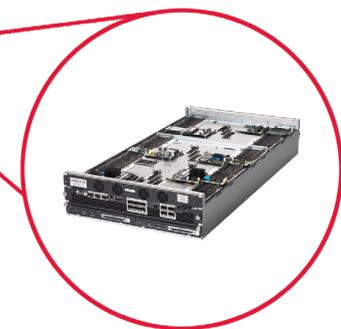
Scalable Capacity

The Cadence Protium X1 platform features an advanced blade/rack architecture, scaling to billions of gates, allowing you to prototype even the biggest AI, machine learning (ML), 5G, mobile, and graphics designs. Each blade can be used standalone or connected to the up to eight other blades in a rack. Multiple racks are connected to realize even larger configurations.

At the same time, flexible, single-FPGA granularity, multi-user capabilities ensure high utilization and efficiency, making it an ideal solution for IoT, automotive, storage, and consumer applications—and, of course, any IP and subsystem configuration. Each blade can accommodate up to six individual users, concurrently running either the same design or completely different designs.

Scalable Performance

Sometimes all you care about is getting the job done as quickly as possible; our AutoFlow, push-button compile, partition, and FPGA place and route (P&R) has you covered. AutoFlow enables you to get to a working FPGA-based prototype in days or week, as compared to multiple months with other FPGA solutions.



Sophisticated performance optimization options allow you to quickly improve the prototyping speed—the more effort one puts in, the more performance one gets!

Sometimes you want the highest possible performance—we have you covered on that, too, with black-box flow in multi-FPGA configurations and our single-FPGA CustomFlow. Both require more manual interaction and design knowledge to achieve best possible performance.

Scalable Debug

While bringing up the design on the Protium X1 platform for the first time, you need comprehensive debug capabilities

to do the job efficiently. Advanced debug features include prototyping full visibility, force and release for internal notes, real-time signal monitoring, and design-memory upload/download.

When deployed for firmware/software validation, features like JTAG and UART integration with software debuggers, clock control (start/stop), memory backdoor access, and assertion checkers are being used.

And when used for high-performance hardware regression and full-system validation, the optional data capture card (DCC) allows you to capture thousands of signals for millions of (user) clock cycles and full prototyping speed.

Flexible Use Modes

Early software development

Successfully completing today’s and tomorrow’s challenging SoC designs, with their ever-increasing software contents, on time and on budget, requires starting the firmware and embedded software development process as early as possible. FPGA-based prototyping has long been a key technology to achieve that goal. However, bring-up of such FPGA-based prototyping systems has been painful and time consuming.

The Protium X1 platform addresses these challenges by providing a comprehensive and productive solution to reduce the prototype bring-up from months to weeks, or even days. Key to this is our powerful FPGA compile and implementation software, which solves the usual FPGA issues, such as clocking, memories, partitioning, and FPGA timing closure, all while preserving the integrity of the original design RTL.

Assemble a Rack

Progress: Add PTMBC cables → Add QSFPCables → Review → Done

Connect QSFPCables

Choose cable length: 3 m (selected) | 10 m

Select either two blades or blade and QSFPC switch, and ports to connect with cable

Legend: Mounted, Not Mounted, Disabled, Unused, Daughter card, IO Board, PTMBC Cables, QSFPC Cables

Rack 1	QSFPC Switch
1	ROC171307632 354 5 5
2	ROC171307632 370 5 5
3	ROC171307632 314 5 5
4	ROC171307632 354 5 5
5	ROC171307632 374 5 5
6	ROC171307632 79 5 5
7	ROC171307632 42 5 5
8	ROC171307632 79 5 5

QSFPC Switch

BLADE ROC171307632

Legend: Used, Available, Disabled, Installed

#	Cable type	Length	Blade	Connector 1	Connector to	Connector 2	Installed	Delete
1	QSFPC	3 m	ROC1713076632	Q-6	ROC1713070000	Q-2	<input checked="" type="checkbox"/>	

Buttons: CONFIRM, BACK, NEXT

Assemble a Blade

Progress: Connect PTMBC cables on blade → QSFPC breakout cards → PTMTC → Add IO boards → Add PTMBC cables → Review → Done

Connect PTMBC cables on the blade

Choose cable length: 425 mm (selected) | 800 mm | 1200 mm | 1600 mm

Select two PTMBC connectors to connect with cable

Legend: Used, Available, Disabled, Installed

#	Cable Type	Length	Connector 1	Connector 2	Installed	Delete
1	VFC56F	425 mm	C-P8	C-P9	<input checked="" type="checkbox"/>	
2	39RP242L	1200 mm	D-Q9	DOQ10	<input type="checkbox"/>	

Buttons: ADD, BACK, NEXT

Full-system validation

With their high speed and external system connections, FPGA-based prototyping systems are a productive solution to allow design teams to validate their IP and SoC designs within the actual system environment. Scalable capacity, high performance, and the availability of a rich Cadence SpeedBridge® adapter portfolio, makes the Protium X1 platform a highly productive system validation solution.

Throughput regressions

As part of their efforts to achieve a “shift left” for software development, hardware verification, and hardware/ software integration, users are adopting a continuum of development engines from virtual prototyping through RTL simulation, acceleration, and emulation to FPGA-based prototyping. The different engines are used both individually and in combinations. Critically important in this use mode is congruency with emulation systems, like the Cadence Palladium® Z1 Enterprise Emulation Platform, including a common compile flow, identical language coverage, and the ability to re-use the Palladium verification environment. The Protium X1 platform is an ideal solution for the project phases in which most hardware defects in the design already have been removed and users must optimize the throughput of regressions at optimized speed and cost points, requiring less interactive hardware debug.

Benefits

Fastest prototype bring-up

- Automatic multi-FPGA partitioning
- Automatic memory compilation and modeling, including support for multi-port memories
- Support for unlimited number of design clocks

Advanced debug

- Waveform capture and storage for off-line debug and analysis
- Signal force and release for interactive debug and design configuration
- Memory upload/download to quickly update design boot image and memory content

- Full clock control including start/stop and run n cycles, enabling advanced verification use modes and automation
- Prototyping full visibility to capture any signal without recompile
- DCC to capture thousands of signals for millions of clock cycles, at full prototyping speed
- Assertions checkers for efficient software debug

Customization through accessories

- Boards are equipped with the most common, standard interfaces
- Expansion connectors for custom and off-the-shelf daughtercards
- Compatible with SpeedBridge adapters
- Support for end-to-end encryption (e.g., to protect third-party IP)

Features

Design input

- Synthesizable RTL (Verilog, VHDL, System Verilog)
- Synthesizable gate-level netlist
- Full support and compatibility with the Palladium series language set (synthesizable constructs only)

Scripting and setup

- Fully scriptable control and runtime
- Runtime graphical user interface (GUI)
- Compatibility with Palladium clock definition files
- Automatic ASIC-to-FPGA memory compilation

Multi-FPGA partitioning

- Fully automatic, multi-FPGA partitioning with FPGA interconnect optimization and FPGA utilization balancing
- Black-box support for high-speed design modules and interfaces
- Automatic clock tree transformation (gated clocks, multiplexed clocks, latches, etc.)
- Automatic pin-multiplexing insertion

Tightly integrated FPGA P&R

- Automatic P&R constraint generation
- Automatic P&R setup
- Support for parallel place and route
- Fully integrated Xilinx Vivado HLx software

Requirements

For compile

- Linux operating system (refer to [Platform Matrix for Cadence Applications](#))
- Minimum of 128GB of RAM
- Minimum of 500GB of free disk space

For control and configuration

- Linux workstation (32-bit or 64-bit; Red Hat or SUSE)
- 64GB of RAM
- 45GB of disk space
- 1 Ethernet port
- 1 USB 2/3 port
- Multiple Protium X1 systems can be controlled from one workstation

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.

Protium X1 Enterprise Prototyping Platform — Blade Configurations		
Description	39RX816V3	39RX816V4
No. of FPGAs	6X Virtex UltraScale VU440-2	
Capacity per blade (design-dependent)	Up to 150M ASIC gates	
Front panel interfaces	10X QSFP+ 2X 4-lane PCIe® Gen3 (1x IPASS, 1x mi+C10niSAS-HD)	
	2X SpeedBridge Adapter Cards	4X SpeedBridge Adapter Cards
Back panel interfaces	4X QSFP+	4X QSFP+
	2X 4-lane PCIe Gen3 (1X IPASS 1X mini SAS-HD) USB host, FPGA JTAG 1X clock-in, 8X clock-outs, 1X est-clock-in	2X 4-lane PCIe Gen3 (1X IPASS 1X mini SAS-HD) USB host, FPGA JTAG 2X clock-in, 32X clock-outs, 1X est-clock-in
On-board interfaces	12X suggested locations for daughtercards (2X per FPGA)	
I/O connectors (PTMBC)	144 connectors (24X connectors per FPGA) Each connector can be configured as 24LVDS + 4 single ended or 52 single-ended signals	
Total user I/Os	3456 LVDS pairs or 7488 single-ended	
GTH connectors (PTMTC)	6X dedicated GTH connectors (one FPGA per connector) 3X shared GTH connectors (two FPGAs per connector) 16X SerDes (16.3Gbps) per GTH connector	
Clock generators	5 programmable synthesizers (2KHz – 945 MHz)	
Blade configuration	Ethernet	
Power requirements	110-240VAC, 50-60Hz, 1000W	
Dimensions	444mm x 131mm x 844mm (W x H x D) 19: standard rack mountable 3U height	444mm x 131mm x 844mm (W x H x D) 19: standard rack mountable 4U height
	Weight	32.2Kg



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