

Cadence Palladium Dynamic Power Analysis

Optimize tradeoffs between power and performance

Cadence® Palladium® Dynamic Power Analysis (DPA) enables system-on-chip (SoC) designers to intelligently identify, capture, and analyze power switching activity for peak and average power analysis. The DPA option uniquely enables engineers using Palladium systems for emulation to also analyze software within the system-level SoC architecture, and perform tradeoffs between power and performance in a realistic system-level environment.

System-Level Dynamic Power Analysis

Palladium DPA offers “what-if” analysis of power consumption based on logic switching activities, with respect to different architecture variations, design implementations, or application scenarios. It allows users to select course-grained analysis over millions of design cycles to generate a power profile, or chose fine-grained analysis to increase accuracy for examining power peaks.

At the system-level, the solution’s ability to run various design or implementation scenarios—and determine their impact on power dissipation under a realistic application environment—is vital to striking a balance between power budget and expected performance.

While the Palladium system has traditionally been used for high-performance functional verification, the new DPA solution extends its emulation computation by generating dynamic power profiles at the system-level. DPA allows system-level engineers to analyze deep

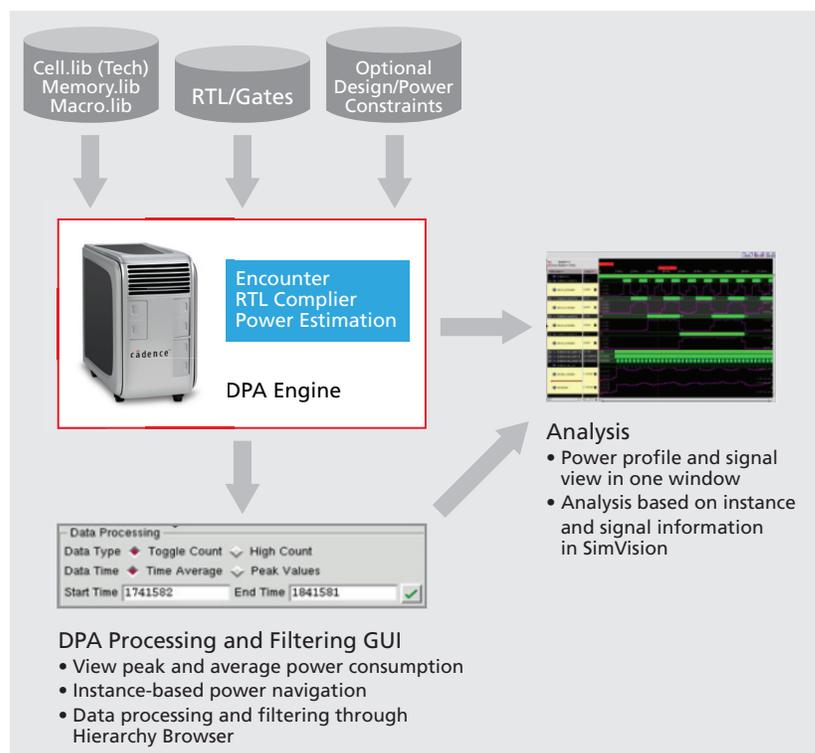


Figure1: Palladium Dynamic Power Analysis user flow

sequences for system-level scenarios typically not practical in a pure software simulation environment.

Additionally, Palladium DPA delivers offline power calculation by capturing the necessary power activities in a common DPA power database. This

capability further enables the sharing of verification resources while DPA is computing the power profile offline.

Power Analysis Flow

Palladium DPA users input RTL or gate-level netlist, along with technology library, memory and macro libraries. The solution also gives them the ability to generate the power profile for a given test. The DPA processing and filtering GUI can be used for identifying a window of interest for further detailed analysis.

Benefits

- Enables system-level power estimation
 - Higher-performance engine
 - Identify peaks
 - Calculate average over long run
- Realistic environment reduces risk
 - Run in-circuit in real environment, full chip, or system-level
 - Run with embedded software
 - Estimates power under real operating conditions
- Detailed analysis on identified windows
 - Identifies where detailed analysis is needed
 - Enables software and/or RTL optimization to reduce power
- Enables relative compare of IP at RTL phase
 - Identify architectural issues
 - Enables hardware/software architectural tradeoffs
- Reduces risk and packaging cost
 - Adequately select package
 - Avoid re-spins/lost opportunities

Features

Peak Identification

- Identifies top N (numbers of) peaks. Each peak is identified by an instance name and time

Average Power Calculation

- Calculates realistic average power based on long simulation runs

Supports Both RTL and Gate-Level Power Estimation

- RTL based power estimation can be used for relative IP comparison
- Gate-level power estimation can be used for more accurate analysis

Weighted Toggle Count

- Weights can be assigned to scale the power consumptions in different elements to the toggle activities. For example, embedded memories consume more power than standard cells for the same number of I/O transitions. Therefore, memories get assigned a higher weight compared to standard cells. This enables more realistic representation of a dynamic power profile.

Toggle Count Analysis GUI

- Enhancements to Palladium debug GUI for Toggle Count Analysis include various data processing and filtering capabilities
- Data processing:
 - Ability to process data in various ways such as toggle count, high count, time average, and peak values
- Filtering:
 - Interval average: This filter will split raw data into intervals of the same size. (Helps reduce the number of windows)
 - Running average: This filter calculates an average number for the selected window. (Helps with a smoother waveform)

Supports the Common Power Format (CPF)

- Allows user to specify advanced power reduction techniques such as power shutoff

Leverages SimVision for comprehensive analysis

- Histogram and filtered data can be viewed along with instance and signals

Specifications

- Requires Palladium III hardware
- Palladium III supported OS and Workstations
 - Solaris (32-bit, 64-bit)
 - Linux (32-bit, 64-bit)
- Includes capabilities of Cadence Encounter® RTL Compiler power estimation and SimVision
- User needs to provide liberty format technology, memory, and macro libraries

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



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