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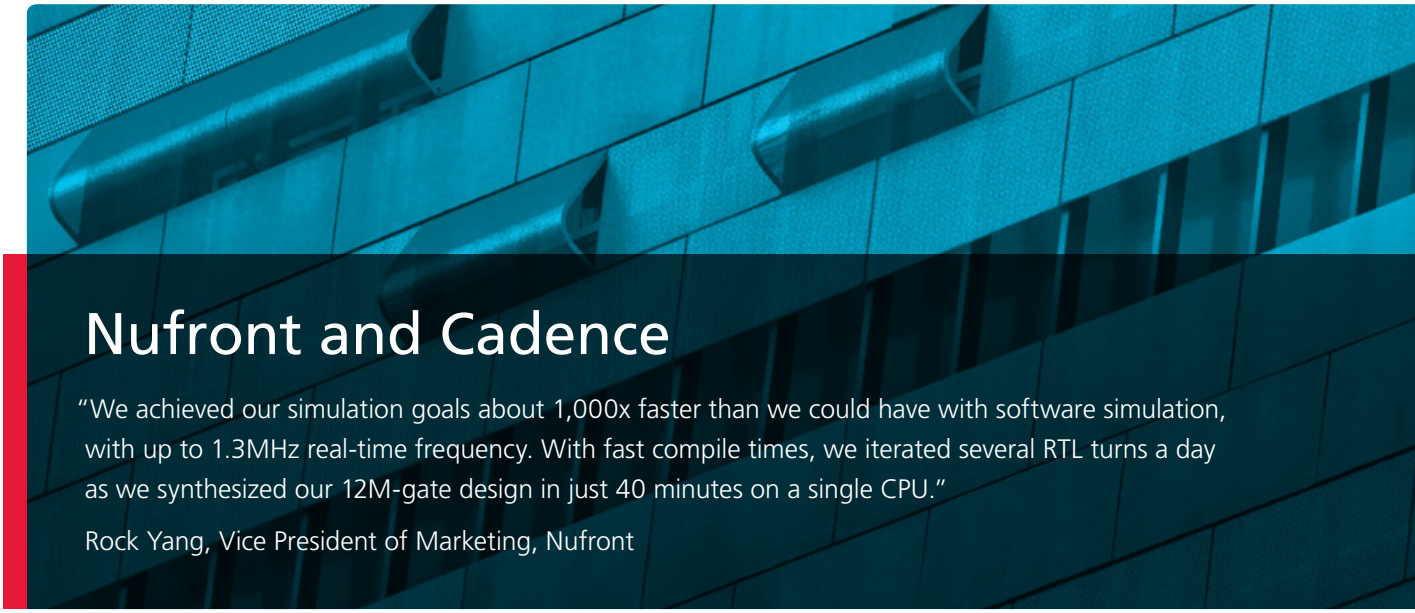

Nufront and Cadence

"We achieved our simulation goals about 1,000x faster than we could have with software simulation, with up to 1.3MHz real-time frequency. With fast compile times, we iterated several RTL turns a day as we synthesized our 12M-gate design in just 40 minutes on a single CPU."

Rock Yang, Vice President of Marketing, Nufront

The Customer

Nufront is a Chinese technology company that develops systems and solutions in the areas of wireless broadband communication and broadcasting, integrated circuit (IC) design, video search, digital-image processing, intelligent transportation, and digital medical. The company expands its reach and capabilities beyond its own research and development (R&D) team by collaborating with industry-leading companies, universities, and academic institutes based in China.

An innovative company, Nufront has been issued approximately 200 patents in the areas of mobile multimedia, wireless broadband, smart central processing unit (CPU) design, video search, and digital-image technology for counterfeit identification and authentication.

The Challenge

Nufront recently introduced its third-generation mobile computing chip, the NS115, which is based on the ARM® Cortex™-A9 dual-core processor. While developing this product, the company had to adhere to strict mobile-computing platform requirements and achieve extremely low levels of power consumption and a high level of performance. The design team's challenge was to verify and emulate the chip with a focus on performance and power with Android applications.

"When we launched this project, a key goal was to build an application-based ecosystem to unite our third-party application vendors and manufacturers," says Rock Yang, Vice President of Marketing at Nufront. "This would increase the value of our chips and enable our customers to speed up product launches and win more business opportunities."

Business Challenges

- Quickly roll out a third-generation dual-core Cortex-A9 mobile computing chip without sacrificing quality
- Enable customers to speed up product launches and win more business

Design Challenges

- Design a complex chip with 12M gates
- Comply with strict mobile-computing platform requirements
- Achieve low levels of power consumption and a high level of performance

Cadence Solutions

- Palladium XP Verification Computing Platform
- Incisive Enterprise Manager
- Palladium XP Dynamic Power Analysis
- SpeedBridge rate adapters

Results

- Sped up simulation goals by approximately 1,000x
- Increased productivity while meeting stringent quality requirements

For example, an ultra-thin 7-inch tablet that uses the Nufront NS115 was recently released on the market. It has a built-in camera interface, high-definition multimedia interface (HDMI) port, and high-definition (HD) video codec with 8.6mm thickness. The device easily supports large-scale 3D games and HD movies. Thanks to the NS115's ultra-low-power consumption, the tablet doesn't heat up during use like many other dual-core tablets on the market.

The NS115 required a complex design with 12 million (12M) gates. It features the ARM Cortex-A9 dual-core processor, which reaches frequencies up to 1.5GHz to meet the operational and performance demands of today's user applications. The design has a dedicated 2D block for hardware acceleration; an ARM Mali™-400 multi-core 2D/3D graphic processor; and numerous memory subsystems and interfaces, including LPDDR2 and DDR3.

The design had to meet Android system requirements, including the need for external storage, multiple screen displays, the ability to accept data input from various sources, and a long lead-time for IC simulation. The Nufront team felt that register-transfer level (RTL) simulation would be too slow for system-level verification, and frequent design iterations and the lack of full debug visibility wasn't suitable to choose a field-programmable gate array (FPGA)-based solution.

"The Cadence solution enabled us to use emulation to analyze software in a system-level environment. We were able to run various design and implementation scenarios and determine their impact on power dissipation in a realistic application environment."

The Solution

Nufront chose the Cadence® Palladium® XP Verification Computing Platform to emulate the NS115, enabling early system-level integration and software validation for Android and Linux while speeding time to delivery and enhancing overall quality.

Using hot-swap technology, Palladium XP increased Nufront's productivity by enabling users to transition among simulation, simulation acceleration, and emulation environments at runtime without re-compilation or re-starts.

The Palladium XP platform integrates with Cadence Incisive® Enterprise Manager to support a metric-driven flow that accelerates verification. Incisive Enterprise Manager automates and manages the execution of regressions on the platform. Nufront engineers were able to use a common verification plan and extract constraint results from multiple locations into a common database for metric analysis.

The Nufront team relied upon Palladium XP for system-level power analysis and power verification. Palladium XP Dynamic Power Analysis enabled them to quickly identify peak and average power of their system-on-chip (SoC) with deep software cycles. During the runs, they identified and zoomed into power peaks with finer granularity to identify the high power consumers in the design. This helped them reduce overall power consumption.

"The Cadence solution enabled us to use emulation to analyze software in a system-level environment," Yang explains. "We were able to run various design and implementation scenarios and determine their impact on power dissipation in a realistic application environment. This allowed us to strike a balance between power budget and expected performance."

To improve verification throughput, Palladium XP offers a hybrid environment that connects it to real-world stimulus through a target or tester and virtual or transaction-based acceleration models. This enables various models to be linked, compiled, or physically connected.

The Cadence solution also allows the reuse of abstracted models such as C/C++, transaction-level models, behavioral RTL, RTL/gate-level netlist, silicon/FPGA/software IP, and system-level interfaces. This enables users to select the highest-performing available IP to integrate hardware and software and improve verification throughput.

Two Palladium XP features that Nufront found particularly useful were the built-in Unified Xccelerator Emulator (UXE) compiler, which improved their compile time, and the ability to expand with the in-circuit acceleration use model that supports both static and dynamic environments.

The Nufront team also appreciated the integrated emulation solution with the Cadence SpeedBridge® family of rate adapters. This enabled them to quickly construct a complete system-level environment that applies real-world system operating conditions, such as booting the operating systems and displaying graphics, prior to the silicon being available.

"SpeedBridge adapters support many industry-standard protocol interfaces that were critical to us during this project," Yang says. "These adapters provided a real-world interface to VGA, UART, SD/MMC, JTAG, and USB peripherals, and they were very easy to use."

Results

Using the Cadence solution, Nufront achieved significant performance improvements and time savings. "We achieved our simulation goals about 1,000x faster than we could have with software simulation, with up to 1.3MHz real-time frequency," Yang says. "With fast compile times, we iterated several RTL turns a day as we synthesized our 12M-gate design in just 40 minutes on a single CPU."

Additional efficiencies of using Palladium XP were immediate and clear to Nufront. "For example, it only took about 15 minutes to boot a RAM file system," Yang adds. "We were also able to refine the Android system so it would boot in about 2 hours versus a projection of 83 days in an RTL simulator."

Summary

By choosing to emulate the NS115 with Palladium XP, Nufront achieved many benefits, including a 1,000x performance improvement over RTL simulation. The company successfully enabled early system-level integration and software validation for Android and Linux using the Cadence solution.

"We successfully correlated power consumption using realistic runtime environments and applications before silicon was available," Yang concludes. "We also achieved a very fast turnaround time, which greatly improved the efficiency of our verification efforts."

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