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NetSpeed and Cadence

The Customer

NetSpeed Systems provides scalable, coherent, on-chip network (NoC) IPs to system-on-chip (SoC) designers for a wide range of markets from mobile to high-performance computing and networking. NetSpeed's NoC platform delivers significant time-to-market advantages through a system-level approach, a high level of user-driven automation, and state-of-the-art algorithms.

NetSpeed developed Gemini, its cache-coherent NoC solution, to address two key limitations in existing hardware-based coherency solutions: performance and scalability. First, coherency systems are usually fixed configurations, which means they cannot adapt to system requirements. They may be over-designed or under-performing. Secondly, to manage the complex on-chip communications, they employ separate interconnects for coherent and non-coherent traffic. These interconnects create unnecessary floorplanning obstacles, prevent efficient resource sharing, require multiple interconnect methodologies, and require additional hardware support to allow the traffic to interact.

NetSpeed Gemini is high performance, scalable, and highly configurable for a wide range of applications. Gemini supports all three levels of coherent traffic—cache coherent, I/O coherent, and non-coherent traffic—in a single NoC.

Business Challenges

In designing a cache-coherent NoC, there is no margin for error. When a deadlock occurs, the system will lock up. Gemini gives customers access to a multitude of configuration parameters that allows them to customize their SoC designs. However, the flexibility of the product allows an endless number of configurations and consequently requires an astronomical number of test cases. NetSpeed needed the ability to perform exhaustive testing without introducing prolonged delays in the development schedule.

Technical Challenges

Long runs are required to hit bugs

Coherency verification is deeply "stateful"—the longer the run, the more states accumulate internal to the chip and the more likely it is to hit corner cases. Contrast this to simpler designs where one long run can be equivalent to many short runs done in parallel; for coherency verification, long runs cannot be substituted with many short runs.

Business Challenges

- Deliver product on time
- Build customer confidence in a new and complex IP product
- Mitigate risks of field failures

Design Challenges

- Provide comprehensive breadth and depth test coverage in a massive verification space
- Provide excellent debug tools and the ability to reproduce problems for rapid resolution of complex failure scenarios

Cadence Solutions

- Palladium® XP series with simulation acceleration and emulation
- Incisive® Enterprise Simulator

Results

- Increased validation speed hundreds of times faster compared to simulation
- Enabled exhaustive test coverage of a massive verification space
- Improved validation team productivity: operations that previously took weeks were completed in minutes

Bugs are deadly and not defeature-able

Coherency bugs are unforgiving. One coherency bug can kill the entire product. Coherency is all about sharing and there is a complex set of protocols to make sure that sharing happens correctly. A bug in any part of the execution can bring down the entire scheme and product. That makes the stakes very high, and the verification more challenging given that long runs are required to discover the bugs.

Vast verification space

Because of the flexibility of configurations for Gemini, some of the additional challenges faced were:

- Providing coverage for a massive verification space, including a large warm-up period, and the capability to expose bugs that manifest only after millions of cycles
- Generating all possible NoC configurations
- Providing an intelligent, coordinated stimulus for the test cases
- Debugging and reproducing errors

The Solution

NetSpeed used the Cadence® Palladium XP acceleration/emulation platform as part of its multi-layered approach to exhaustively verify Gemini. NetSpeed decided on a "depth and breadth" verification strategy that used Cadence Incisive simulation to quickly cover large numbers of configuration and emulation to validate complex time-dependent scenarios. The Palladium XP platform allowed NetSpeed to run more realistic workloads and to test more complex SoC power interactions that are not possible in simulation. Self-checking stimulus loaded onto Palladium XP platform enabled running billions of instructions, which enabled NetSpeed to reach further faster and flush out any elusive bugs. Furthermore, the methodology enabled NetSpeed to replay emulation runs in Incisive simulation, matching every cycle between the two. NetSpeed used the Palladium XP platform to find long and complicated bugs, and the ability to replay and debug in a timely manner proved especially crucial.

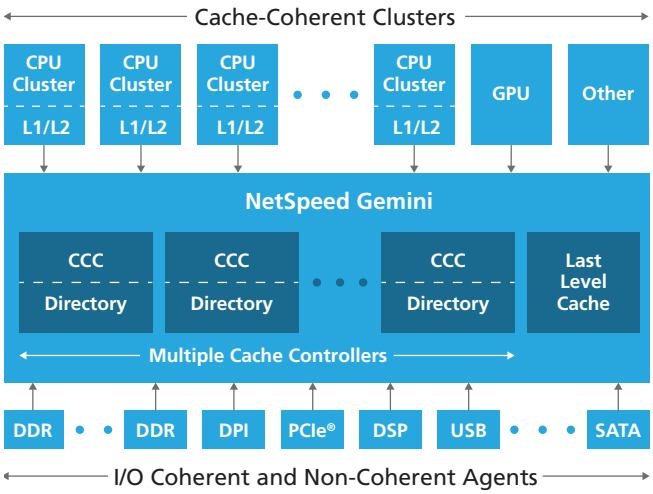

Figure 1: NetSpeed Gemini NoC Solution

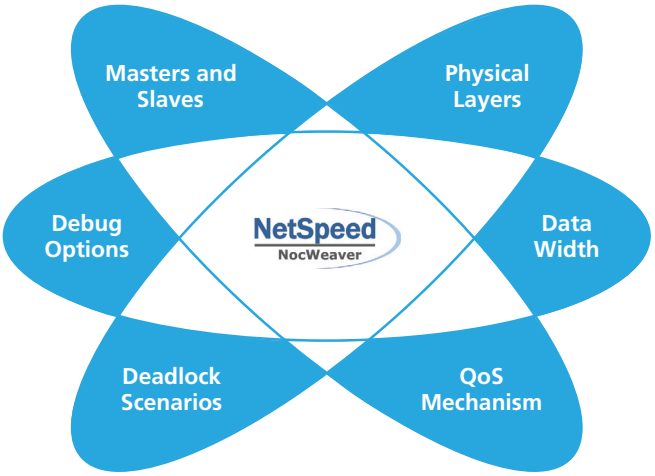

Figure 2: NetSpeed NocWeaver

NetSpeed used its in-house NocWeaver software to generate more than 1000 NoC designs every night. Using the Palladium XP platform, NetSpeed was able to run much longer, exhaustive tests. Implementation and bring-up of the Palladium testing environment took less than a week. Testing that would normally have spanned weeks to complete was done in minutes.

Summary and Future Plans

The Palladium XP platform is an integral component of NetSpeed's overall solution for verification challenges. NetSpeed plans to use the Palladium XP platform on future product releases because it enables comprehensive testing that would otherwise be infeasible. The Palladium XP platform mitigates business risk and helps to build customer confidence in NetSpeed's products.

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