cadence®

Metric-Driven Mixed-Signal Verification Flow

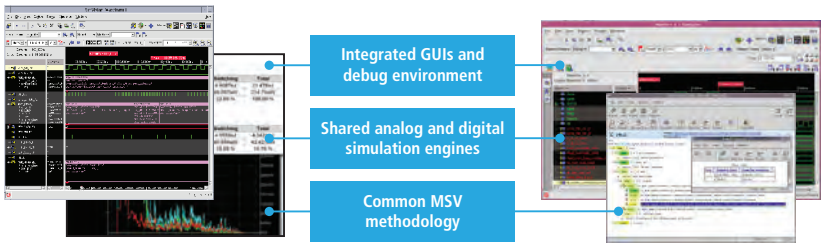
High-performance, top-level verification for reliable mixed-signal designs

Cadence provides a metric-driven mixed-signal verification (MSV) flow for customers who employ digital-centric use models for high-performance MSV to enable full-chip verification. The flow enables MSV very close to digital speeds, and can be used for high-volume, digital-centric nightly regression runs.

MSV Flow

The old mixed-signal world looked like an analog environment on the left bolted to a digital environment on the right. Depending on which engineering group was responsible for final assembly, one part would be treated as a black box and the two parts would be bolted together at the system-on-chip (SoC) level. But today's mixed-signal designs have multiple feedback loops, complex modeling requirements, and higher performance targets, meaning it's no longer possible to deconstruct designs into separate analog and digital functions. Engineers must embrace the digital-centric metric-driven verification methodologies into their MSV flows. Engineers also need an integrated MSV environment that focuses on performance and reliability. Top-level SoC verification has become a critical challenge—and functional failures can result in costly design iterations and missed market windows.

Mixed-signal design and verification environments are not an entirely new ballgame. In the broader context, from an analog perspective, engineers have been doing mixed-signal design for years; however, it seems today that



neither analog nor digital engineers are completely prepared to enter each others' areas of expertise. Analog engineers may shy from the complexity of SoC verification, and digital engineers may find the fuzziness of analog design disconcerting in the context of applications that must run on the chip. However, there's simply no way to avoid this interaction. Functional integration is the key problem.

To address the functional integration problem at the SoC level, customers should start with a verification plan. Verification planning is the process of using the specification to define what to check, not looking at the design and defining how to check. By planning what to check, the engineer makes sure that all the features that are expected at the SoC level—not just what's designed into the block—are covered. This is a major failure area in mixed-signal SoCs in that the analog block is verified under different conditions at the SoC level than at the block level. Verification planning is one of the key steps to managing the complexities involved in the digital-centric mixed-signal (DMS) verification flow.

Planning translates into coverage, assertion-based checking, and score-boarding as well as appropriate stimuli generation for both digital and analog components. The planning process is always important for verification, but for mixed-signal it is critical. The sheer range of operating parameters and complex interaction of analog and digital units requires a clear definition of relevant metrics defined and measured for all units. Traditionally, there has been very little functional coverage collected from

within the analog domain. Now, it is possible to include analog parameters as part of the coverage models when using the DMS verification flow. Key metrics and targets for functional completeness of the DMS effort are captured in an executable specification often called the vPlan, which attaches itself to the verification environment. As simulations are run, the coverage information is collected and annotated into the vPlan to give a graphical representation of the percentage coverage achieved.

Driving MSV into SoC Regressions

The Cadence® MSV flow leverages real-number modeling (RNM) so that users can perform top-level verification of their analog or mixed-signal designs using discretely simulated real number models. First introduced by Cadence as wreal models, RNM provides the digital equivalent model of an analog block, enabling engineers to verify a full-chip SoC using only a digital simulator. This eliminates relatively slow analog simulation and convergence issues, allowing for nightly regression runs of the mixed-signal SoC. RNM has recently gained increased popularity through support for SystemVerilog IEEE 1800-2009, and SystemVerilog Discrete Real Modeling Committee (SV-DC) IEEE 1800-2012 capabilities. These new capabilities are driving rapid adoption of chip-level MSV. RNM can also integrate with other advanced verification technologies, such as assertion-based verification and metric-driven verification without having to interface with the analog engine or defining new semantics to deal with analog values. Using the Cadence MSV flow, engineers can greatly enhance the top-level verification performance of the overall verification process.

Flow Benefits

- Improves time to market
  - Overnight mixed-signal regression runs ensure the chip meets the specification
  - Ensures product quality
- Reduces re-spins
  - Leverages high-performance RNM
  - Performs SoC top-level MSV
  - Finds and fixes errors much earlier in the design cycle by performing full-chip functional verification
- Boosts productivity
  - Eliminates convergence issues with digital-speed performance
  - Easily and accurately ports models between Virtuoso® and Incisive® environments
  - Enables top-level SoC verification

Flow Components

- Incisive Enterprise Simulator with DMS Option
- Virtuoso AMS Designer Simulator
- Virtuoso Multi-Mode Simulation

Real Number Modeling Specifications

- SystemVerilog IEEE SV-DC 1800-2012, including:
  - User-defined types (UDTs)
  - User defined resolution (UDRs)
  - Explicit interconnects
- SystemVerilog IEEE 1800-2009, including:
  - Real-number variables
  - Input/output real ports
  - Assign statements to real variables
  - SVA assertions including real variables
- Basic wreal modeling
  - Wreal declaration
  - Local use of wreal declaration in behavioral construct
  - Hierarchical connection of nets with explicitly assigned wreal type
- Advanced wreal modeling
  - Multiple wreal drivers
  - Global and scope-based wreal drive resolution
  - wrealXState and wrealZState
  - Wreal table models
  - Wreal arrays
  - Hierarchical connection
  - Real assertions
  - AMSD block (no analog engine)
  - R2L/L2R (digital only with no mixed-signal, mixed-language interactions)
  - Wreal to SV real

NOTE: For full language support, see Incisive Enterprise Simulator datasheet

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