cadence®

Memory Model Portfolio for Palladium Series

Rapid system-level verification deployment

The Cadence® Memory Model Portfolio is a pre-validated system-level emulation solution that provides memory device models for Cadence Palladium® series. An off-the-shelf plug-and-play library, the models in the Memory Model Portfolio enable rapid deployment of high-performance system-level emulation by providing an extensive array of high-quality synthesizable models for industry-standard memory devices that are widely used in networking, storage, wireless, and multimedia applications. The Memory Model Portfolio allows users to leverage complex state-of-the-art memory and storage protocols without tying up engineering resources, thus improving validation productivity.

Pre-Validated, Off-the-Shelf Emulation Memory Solution

As the speed and flexibility of technologies grows, so does the complexity of modeling each memory technology. As an off-the-shelf emulation solution for designs with storage and memory requirements, the Memory Model Portfolio for Palladium series is a pre-qualified solution that offers synthesizable models of high quality for easy integration. Leveraging Cadence's emulation and memory protocol expertise facilitates a faster path to a sophisticated system-level verification platform.

Today's complex SoCs rely on several different memory technologies. As shown in Figure 1, the Memory Model Portfolio addresses these storage requirements with a wide-ranging array of industry-standard models covering all major memory storage families. Whether the applications in your system-level design include DRAM for large external memory subsystems, NAND Flash for booting a Linux OS, SPI for bootstrap code, an

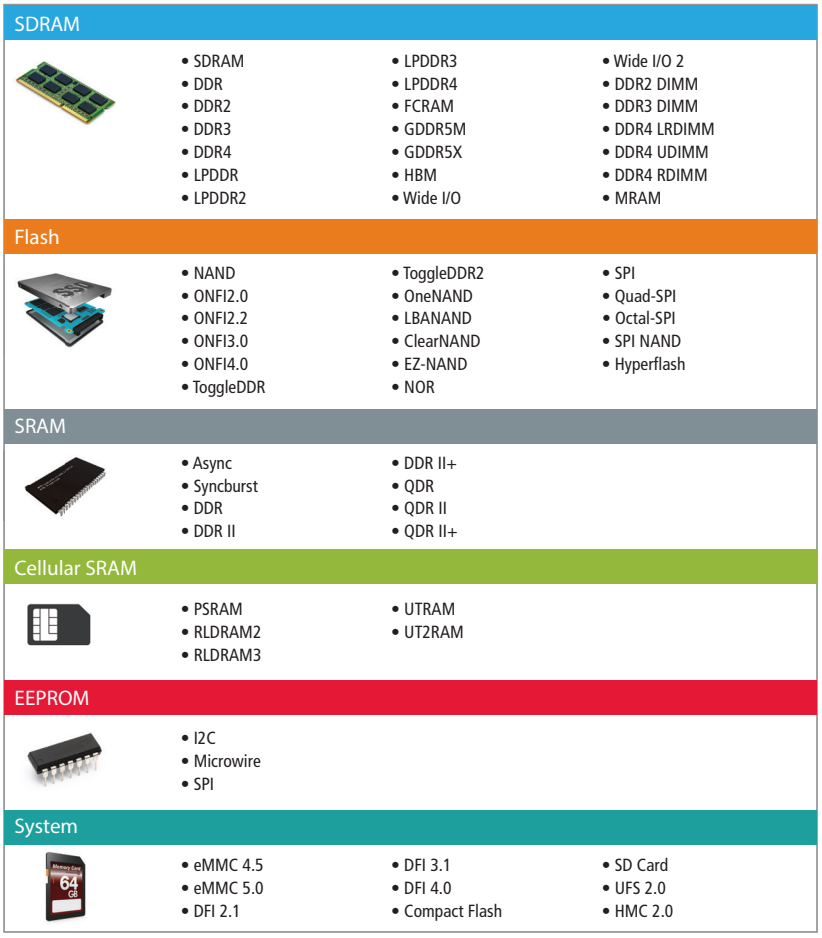

Figure 1: The Cadence Memory Model Portfolio offers an extensive set of models for advanced system-level verification.

SD Card for removable system flash—or all of the above—this emulation-ready library provides project solutions for you.

For system-level validation, the Palladium series along with the Memory Model Portfolio support a design team in rapidly constructing a complete emulation environment that applies real-world system operating conditions to the design. Whether your design requires transferring files, displaying graphics and video, or booting an operating system, the components of the Memory Model Portfolio integrate seamlessly in place of industry-standard devices that are widely used. Once models are selected, users can easily bring-up and configure their Memory Model Portfolio library components, then compile and run with the extensive FullVision design debug capabilities of the Palladium series.

Benefits

Simplifies and speeds verification deployment

- Provides an extensive pre-validated library of emulation models fully compatible with the Palladium series
- Enables rapid creation of system-level environments using memory models tuned for ease of adoption
- Offers widest selection of SoC and system-level memory models
- Models real memory parts and devices
- Provides memory-related IP like DFI PHY and CAMs

Enables verification IP reuse

- Built to specifications of real industry parts and standards-compliant devices and protocols
- Eliminates redundant implementation of memory models customized for each project verification environment

Ensures quality

- Leverages Cadence expertise and knowledge in memory modeling for emulation and acceleration
- Developed and tested by Cadence then qualified by Cadence in real user designs
- Mature memory modeling technology deployed in many emulation environments over many years

Highest performance with the least abstraction

- Tuned for high-end, cycle-accurate performance during system-level verification
- No co-simulation required; performance efficiency not degraded by behavioral constructs
- Optimized for emulation capacity
- Offers best-in-class verification performance without abstracting out critical functionality

Reduces system risk

- Cadence-provided solution assists you in verifying your design quickly and efficiently

Instrumentation facilitates debug

- Popular models equipped with reference waveforms as well as debug-mode messaging for states, accesses, and errors

Features

- More than 800 models across major device families and vendors
- Fully synthesizable with minimal gate capacity usage
- Uses memory resources internal to the emulator
- Time-intensive functions internally clocked and optimized for fast completion
- Eliminates detailed timing and constrains protocol checking to achieve best emulation and acceleration performance
- Developed, tested, and qualified by EDA company or memory vendor
- Popular models include reference waveforms and a $display-based debug mode
- Targets acceleration, transaction-based acceleration, synthesizable testbench, and in-circuit emulation use models

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet. They can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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