Practical ECOs using Conformal ECO tool
Marvell at a Glance

- Founded in 1995
- Top 5 fabless semiconductor company
- A total solution provider: Leader in storage, cloud services and infrastructure, connectivity, communications and consumer products
- Ship ~1 billion chips per year
- 7000+ employees worldwide
- 3200+ patents, > 3000 patents pending
- Industry standards leadership
Marvell Portfolio

- Cloud services and infrastructure
- Smartphones and tablets
- Smart TVs, set-top boxes, Blu-Ray players
- Connected displays and printers
- Enterprise and home networking
- Smart home appliances
Mobile and Wireless

- **Wireless**
  - Fully-integrated SoCs featuring Wi-Fi, Bluetooth, GPS, FM and NFC in a single small package
  - Industry leader in wireless printers and gaming

- **Communications/applications processors**
  - Integrated, total system solution for gaming, mobile phones, tablets and printers
  - Leading-class performance for voice and computation-intensive data applications
  - TD-SCDMA, WCDMA, LTE
  - Ultra-low power processing, higher performance, and full software compatibility

- **Software**
  - Kinoma, an open source software platform for a fully integrated mobile solution

From Wi-Fi to TD-SCDMA our mobile solutions enable devices that connect people anytime, anywhere on any screen.
Motivation for Automated ECO flow

• Implement design changes in an automated fashion in reasonable amount of time after RTL freeze.
• Typically multiple ECOs are done on every project late in design cycle.
• Complex ECOs are hard to implement manually.
• Existing formal verification flow can be leveraged with minimal changes for conformal ECO flow.
• Has ability to Post mask ECOs with spare gate, with physical and timing information.
• Improve the productivity by reducing the time taken in ECO phase.
Conformal ECO handles large and complex ECOs fast, RTL2 to LAY2 converges faster

*Use your preferred implementation tools
## Conformal ECO Steps

<table>
<thead>
<tr>
<th>Step Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 vs R2</td>
<td>• Compare LEC golden RTL and Modified RTL.</td>
</tr>
<tr>
<td></td>
<td>• Review the non-equivalence points.</td>
</tr>
<tr>
<td>R1 vs LAY1</td>
<td>• Compare Golden PNR netlist with original RTL. This should be clean.</td>
</tr>
<tr>
<td>R2 vs G2</td>
<td>• New RTL with ECO fix compared with synthesized netlist of R2 for equivalence. This should be clean.</td>
</tr>
<tr>
<td>LAY1 vs G2</td>
<td>• Non-equivalence expected. Compare this non-equivalence with step 1.</td>
</tr>
<tr>
<td>Generate the ECO</td>
<td>Analyze ECO step to generate the patch. Apply the patch to LAY1.</td>
</tr>
<tr>
<td>LAY1+patch vs R2</td>
<td>This should be equivalent.</td>
</tr>
</tbody>
</table>
The flattened ECO flow is a simplified ECO flow with the following benefits:

- Supports hierarchical clock-gating cloning/decloning, inverter pushes, and boundary optimization for hierarchical designs.
- Focuses ECO analysis on non-equivalent (NEQ) key points identified from a flat compare.
- Can select and choose which design module to run the flattened ECO flow.
- Offers on-demand insertion of ECO pin/ports through an ECO pin dofile (adds ECO pins to only the NEQ ECO cones).

Easier set up
- Creates all ECO patches with one command.
- A hierarchical run is not required.
Conformal ECOs at Marvell during pre-mask stage.

We have done multiple ECOs using Conformal automated flow on various projects for the past few years. Below is the data for

• Example 1 – Block A – Pre-mask ECO was done inside a control block which was instanced multiple(12) times. ECO fix involved combinational logic change in control block. Without automated flow the fix would have been near to impossible to do.

• Example 2 – Block B – Pre-mask ECO involved RTL changes due to wrong address signals connected to address decoding logic. The logic was merged and optimized out during synthesis. The ECO patch involved new combinational logic and flop additions. The fix would have been very difficult to do this manually as the logic got optimized out. With automated flow it was done very easily. The only limitation of the tool is addition of new flops into existing scan chain.

• Example 3 – Block C – Pre-mask ECO involved control logic change repeated at 32 different places. Tool could identify common RTL change at multiple places and came up with optimized patch for this case.
## Pre-Mask ECO Results

<table>
<thead>
<tr>
<th>Design</th>
<th>Size</th>
<th>ECO FIX in RTL</th>
<th>Patch Size</th>
<th>Run Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block A</td>
<td>500K</td>
<td>Modify two conditions in a big IF statement for sequential logic.</td>
<td>For one instance (multiplied by 12 for 12 instance) – 9 library cells are added in the patch. 2 library cells removed from the existing logic</td>
<td>661 sec</td>
</tr>
<tr>
<td>Block B</td>
<td>178K</td>
<td>Modify logic for 4 DFF Add 2 new DFF Modify 7 assign statements</td>
<td>2 DFF added 10 Library cells added</td>
<td>420 sec</td>
</tr>
<tr>
<td>Block C</td>
<td>2K</td>
<td>Change address decoding logic - which involved modification of same condition at 32 different places.</td>
<td>1 library cell added</td>
<td>466 sec</td>
</tr>
</tbody>
</table>
Conformal ECO Handles Standard Cell Spare Gates

• In addition to pre-tapeout ECO handling, Conformal ECO Designer also automates ECOs for spare cell optimization and mapping.

Standard cell spare gates considerations:
• DEF is used to derive
  – Spare cell types and instance quantities
  – Spare physical location
• LEF also used
• In addition to technology mapping, Conformal ECO
  – Maps ECO logics to spare & freed up gates
  – Considers spare gate’s physical location
  – Reports inadequate spare cell resources
Post Mask ECO

Below is an example of post mask ECO using only existing spare cells on metal only stepping

• Block A – This Post Mask ECO involved combinational logic change. The fix needed to be changed using only spare cells and metal layers. In this ECO we used the physical and timing information to generate the patch. The BE implementation took only one iteration without introducing any timing issues.
## Post Mask ECO results.

<table>
<thead>
<tr>
<th>Design</th>
<th>Size</th>
<th>ECO FIX in RTL</th>
<th>Patch Size</th>
<th>Run Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block A</td>
<td>725K</td>
<td>Change two “IF conditions” in a sequential logic. Add one new condition and change the existing condition.</td>
<td>Added 4 spares cells into the logic. Redo some of the existing Logic.</td>
<td>542 sec</td>
</tr>
</tbody>
</table>
Conclusions

**Positive Points:**

- Able to handle complicated ECOs involving combination and sequential fixes with ease.
- Able to handle adding new DFF as part of the ECOs.
- Can do pre or post mask ECOs.

**Limitations:**

- Limitation of tool to insert the newly added DFF into existing scan chain.
- Trade off between productivity and getting the most optimal patch.
- Would be nice to use R2 rather than SYN2 for patch generation to improve the overall timing of the ECO flow.
Acknowledgements.

• Would like to thank Cadence AEs for excellent support in resolving issues faced during ECO implementations with scripts and developing the flow for pre & post mask ECOs.