cādence®

Incisive Verification Apps

Formal and simulation approaches to solve common verification challenges

With a combination of formal, simulation, and metric-driven technologies, the Cadence® Incisive® Enterprise Verifier's hybrid approach allows the appropriate technology to be applied to design verification closure, and the contribution from formal and simulation techniques can be clearly illustrated using metrics familiar to the verification team. Verification apps, including Super Linting, Protocol Compliance, Coverage Unreachability Analysis, Register Map Validation, and SoC Connectivity apps, apply these technologies to the challenge of unfamiliar analysis workflow and unpredictable tools, as well as providing methods to automate property generation for a given verification task.

Formal Verification Challenges

Formal verification tools combined with SVA or PSL properties yield an exhaustive solution to a wide range of verification challenges. Despite this, formal verification is still often viewed by design and verification managers as something of a "black art"—the preserve of a small group of expert users. The challenges these managers cite as barriers to wider adoption of formal verification commonly include:

• Formal analysis workflow and reports are unfamiliar, so verification leads sometimes struggle to show the full value of formal techniques

• Formal tools exhibit run-times and capacity needs that are sometimes difficult to predict for verification engineers and managers used to traditional simulation-based techniques. Careful qualification is required to identify blocks that benefit from formal versus simulation techniques, often leading to a perception that formal techniques do not scale easily
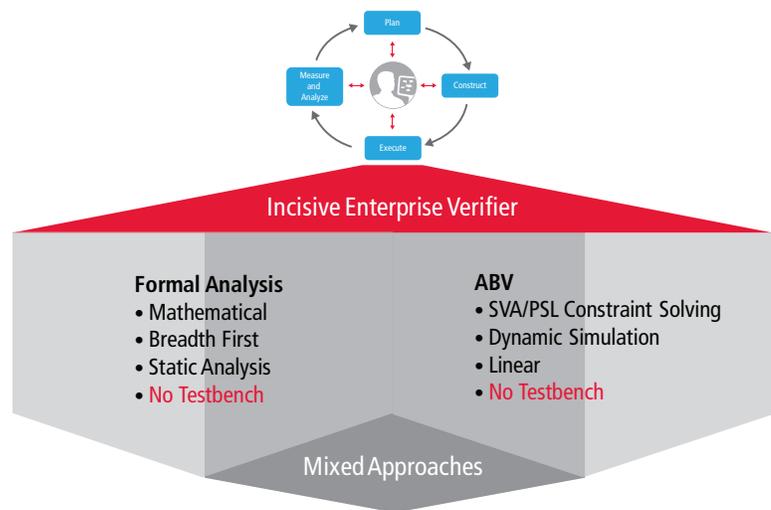

Figure 1: Incisive Enterprise Verifier provides a hybrid approach to verification

• Many engineers—especially designers—are resistant to learning assertion languages and writing properties manually

The first two issues can often be addressed effectively by employing a combination of formal, simulation, and metric-driven technologies. As shown in Figure 1, Cadence provides such a range of technologies in the Incisive Enterprise Verifier.

This hybrid approach allows the appropriate verification technology to be applied to the problem in hand, and the contribution to verification closure from formal and simulation techniques can be clearly illustrated using metrics familiar to the verification team. Verification apps apply these technologies appropriately, and additionally provide methods to automate property generation for a given verification task, to mitigate all three of the formal verification adoption challenges.

The Apps Approach

To bring formal and assertion-based verification (ABV) tools and techniques into mainstream use, a whole new approach is needed—one that puts the focus on the verification problem to be solved, rather than the attributes of the technology used to solve it. As such, Cadence has created the "verification apps" approach, which is defined by the following principles:

- A verification app is a well-documented methodology supplemented by dedicated tool capabilities focused on a high-value solution to a specific verification problem

- A verification app uses the appropriate combination of formal, simulation, and metric-driven technologies, aimed at solving the given problem with the highest efficiency

- A verification app provides significant automation for creating the properties necessary to solve the given problem, reducing the need for deep ABV expertise, and easing deployment

- A verification app provides customized debug capabilities specific to the given problem, saving considerable time and effort

Benefits

- Apps quickly solve painful, high-value problems

- Apps are designed for formal/ABV novices to quickly set-up and run

- Many apps tie into metric-driven verification (MDV) flows, making formal/ABV relevant to simulation-centric managers

- Starting from scratch, real results can typically be seen in a matter of hours, sometimes even minutes

- Once integrated into a verification team's workflow, apps tend to proliferate among engineers on their own, freeing up valuable CAD-team support resources
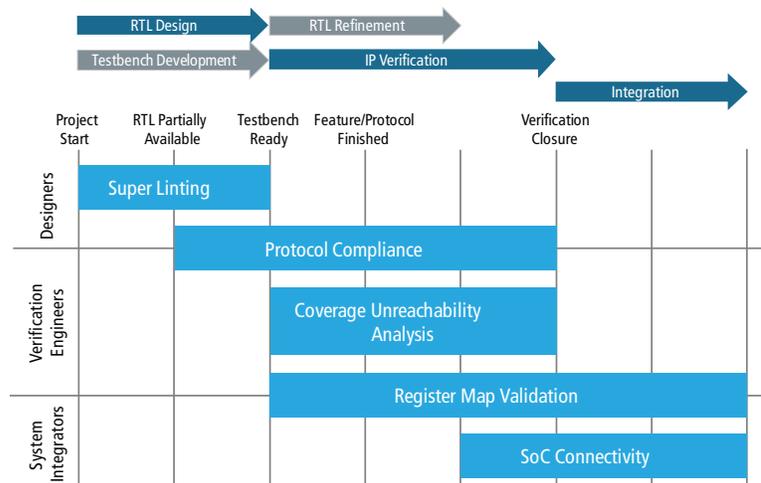

Figure 2: Incisive verification apps span the project life cycle

Availability

As illustrated in Figure 2, Cadence currently ships a variety of apps, including Super Linting, Protocol Compliance, Coverage Unreachability Analysis, Register Map Validation, and SoC Connectivity, that span the entire project life cycle.

As shown in the diagram's Y-axis, users gravitate toward apps that address high-value problems in their particular domains. But since running the apps doesn't require any knowledge of formal verification or ABV, users of all types get results quickly. These results are automatically translated and fed into the metric-driven planning, management, and verification flow in Incisive Metrics Center and Incisive Enterprise Manager, which are familiar to simulation-centric colleagues and managers.

Verification App Highlights

Super Linting

The Super Linting verification app builds on the automatic formal analysis (AFA) capability, in which Incisive Enterprise Verifier (or Incisive Formal Verifier) automatically generates properties from implied behavior of the DUT's RTL. With these properties, the tool runs a variety of automatic checks including deadcode, FSM, X-propagation, and more. The Super Linting GUI overlays the results of the Incisive HDL analysis and linting (HAL) tool with the data from automatic formal analysis to provide a complete picture of the static analysis of your DUT mapped directly to the RTL source code browser. This data is presented in common, easy-to-understand reports. Additionally, the Super Linting app provides the easiest way for designers to get involved with the ABV process.

Figure 3: Super Linting verification app

Protocol Compliance

The Protocol Compliance verification app is based on a library of protocol-specific assertion-based verification IP (ABVIP). Part of the Cadence Verification IP (VIP) Catalog, the Protocol Compliance ABVIP is a library of interface properties is available to validate interface protocols like ARM® AMBA® APB™, AHB™, AXI™ 3, AXI 4, ACE™, OCP, and the DDR3/4 PHY Interface (DFI). These properties are written in IEEE-standard SVA to support both simulation and formal flows. Among the benefits of these pre-packaged property libraries are fast bring-up (just
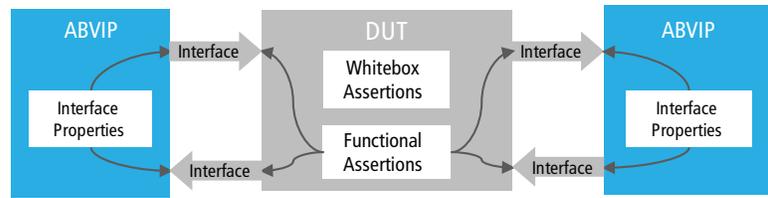

Figure 4: Protocol Compliance app using ABVIP

instantiate and configure), minimal debug of missing constraints, protocol-aware debug in SimVision with transaction-level views, and quick sanity checks and coverage points. When used with Incisive formal and multi-engine tools, this

ABVIP enables users to quickly bring-up designs and exhaustively verify protocol compliance without a testbench.

Coverage Unreachability Analysis

Holes in code coverage can take weeks to analyze manually, to confirm whether they are unreachable (UNR). With the Coverage Unreachability Analysis app, this previously tedious, time-consuming, and error-prone process is completely automated. Properties are generated automatically from holes remaining in the simulation regression coverage database, so users can tell at a glance whether code coverage holes are reachable or literally impossible to hit.
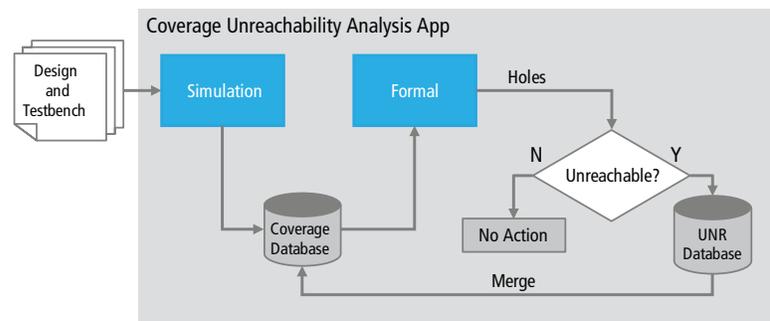

Figure 5: Coverage Unreachability Analysis app

Register Map Validation

Correct register map access and absence of corruption is not checked sufficiently in simulation. By using the Register Map Validation app to generate properties automatically for your SPIRIT/IP-XACT specification, you can exhaustively check a multitude of common register use cases like value after reset, register access policies (RW, RO, WO), and write-read sequences with frontdoor/backdoor access. All these sequences are shown in clear, easy-to-use debug views.
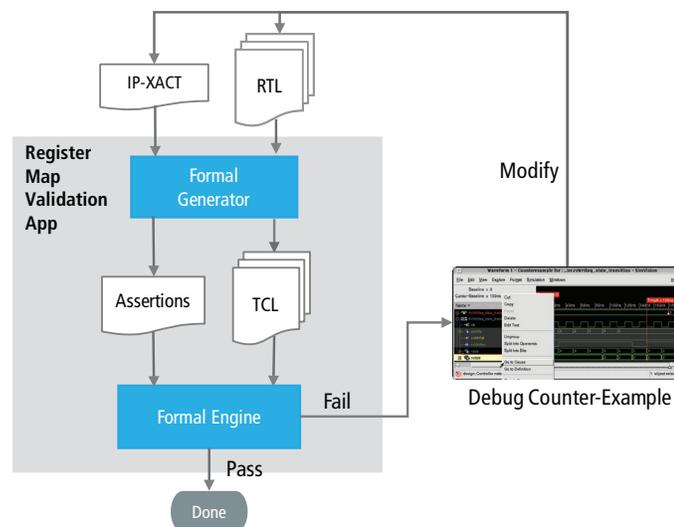

Figure 6: Register Map Validation app

SoC Connectivity

Modern system-on-chip (SoC) designs can have more than 1,000 unique IP components. Even the once-simple pad ring block can have dozens of multiplexed channels that each support out-of-band use cases like BIST and low-power control. Creating a testbench for all of this connectivity is time-consuming and error-prone.

The SoC Connectivity app leverages your design specification to automatically generate and verify properties. Schematic-level debug views are provided. Users of this app commonly achieve interconnect verification within hours instead of weeks or months.
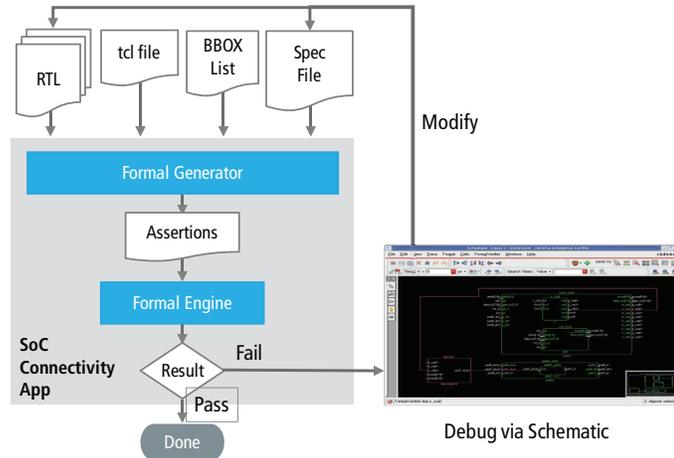

Figure 7: SoC Connectivity app

Other Applied Uses of Incisive Formal Technologies

Incisive Verification apps provide a level of automation and maturity enabling non-expert deployment of solutions for a number of widely occurring verification problems. There are many other documented use models for applying Incisive Formal technologies to solve complex verification problems.

While other vendors may refer to similar use models as "apps", these have not yet reached the level of general repeatability to be called Incisive Verification Apps, but may in the future. These include:

- Security: Verifying the correct protection of secure data and resistance to threats

- Low power: Techniques that complement capabilities in Incisive and Encounter® Conformal® products

- Datapath verification: Exhaustive data transport verification

Cadence also regularly works with verification engineers to create custom apps that address their company's unique verification needs and workflows. Please contact us with your questions and ideas.

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training

- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom

- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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