

# Incisive Enterprise Verifier

Integrated formal analysis and simulation engines for faster verification closure

With dual power from integrated formal analysis and simulation engines, Cadence® Incisive® Enterprise Verifier allows designers, formal verification experts, and dynamic simulation verification engineers to bring up designs faster, begin bug hunting earlier, and gather more metrics toward verification closure by simultaneously leveraging SVA, PSL, code, and functional coverage analysis.

## Incisive Enterprise Verifier

Incisive Enterprise Verifier delivers dual power from tightly integrated formal analysis and simulation engines. Specifically, it includes all of Incisive Formal Verifier and Incisive Enterprise Simulator XL, leveraging both to offer unique new multi-engine integration capabilities. With easy set-up and automatic operation for most users, supplemented by fine-grain controls for experts, Incisive Enterprise Verifier increases return on investment in assertion-based verification (ABV). Additionally, with the ability to automatically translate formal results into dynamic simulation terms, Incisive Enterprise Verifier seamlessly combines the strengths of each technology in a true metric-driven verification flow.

Since Incisive Enterprise Verifier does not require a testbench, you can bring up your design much sooner and begin verification months earlier when designing RTL blocks. It also provides support for metric-driven verification across the enterprise, with verification planning, regression operations on server farms, consolidated formal and simulation metrics, and multi-core performance capabilities

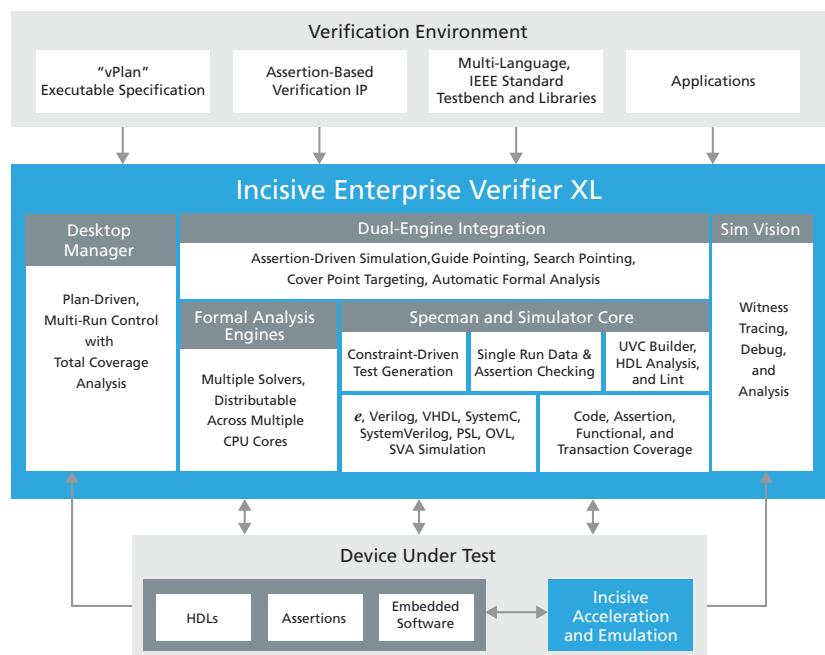


Figure 1: Incisive Enterprise Verifier combines unique multi-engine formal and dynamic simulation capabilities with Incisive Formal Verifier, Incisive Enterprise Simulator XL, SimVision, Desktop Manager, and built-in support for assertion-based verification, the Universal Verification Methodology (UVM), and metric-driven verification

The pure formal verification engines inside Incisive Enterprise Verifier use the industry's most advanced formal analysis technology to offer teams superior performance, capacity, and ease of adoption, which leads to

reduced block debug and integration time. Coupled with the embedded simulation technology of Incisive Enterprise Simulator XL, engines and metrics from both worlds are combined in unique ways to enable

significantly deeper state space exploration than is possible with any single engine alone.

Additionally, Incisive Enterprise Verifier can derive dynamic simulation stimulus and constraints from your assertions, giving you directed tests to replay in dynamic simulation to bring up your design faster. The net result is significant gains in your productivity, predictability, and end-product quality; all of which minimizes your risk of re-spins and accelerates your time to market.

## Benefits

### Better schedule predictability

- Drives the entire verification process from plan to closure with the vPlan executable specification
- Ensures a more consistent verification process by applying mutually reinforcing metrics from both formal and dynamic simulation in an automated, metric-driven verification flow

### Increased productivity

- Uses the familiar and flexible SimVision GUI to support novices and experts alike, with witness tracing and other simulation synergies for ease of adoption
- Designers can start verification months earlier, before the HDL testbench is even specified
- Verification engineers can leverage the mix of dynamic simulation and formal analysis capabilities to reach signoff faster
- Reduces block design effort and debug time, and shortens hierarchy integration time
- Automates generation, assertion checking, and functional and code coverage to provide a “total coverage” view
- Supports IEEE standard languages for easy reuse

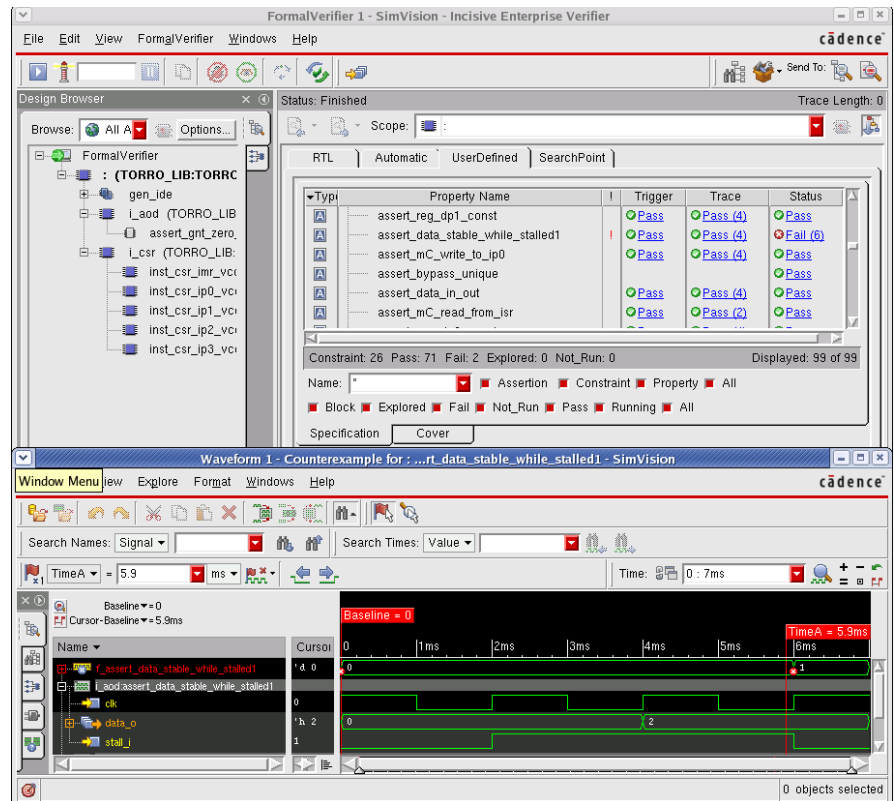


Figure 2: The familiar SimVision integrated debug environment is the basis of the Incisive Enterprise Verifier GUI; novices can rapidly adopt pure formal and dual-engine technologies while experts have a rich superset of capabilities that give them the added control they desire

### Enhanced end-product quality

- Mutually reinforcing metrics improve quality and reduce risk of re-spins by exposing corner-case functional bugs that are difficult or impossible to find using either pure formal or dynamic simulation methods alone
- Reduces the time to discover and correct logic and transaction modeling errors via an integrated graphical debug environment

simulation begins. With this approach, bugs are detected much earlier in the design cycle and are easier and significantly less costly to fix. As the project progresses, the same assertions travel with the blocks and are verified by simulation, acceleration, and emulation later in the design cycle, with all the metrics being combined into a unified view for a true, total coverage picture. This effectively leverages the strengths of all the technologies to further improve quality.

## Features

### Built-in methodology support

Incisive Enterprise Verifier is an integral part of a comprehensive assertion-based verification (ABV) and metric-driven verification (MDV) flow. For maximum efficiency, different technologies need to be used where their strengths are maximized. For example, formal analysis is deployed at the beginning of the verification flow as the designers write RTL and assertions—months before testbench

### Executable verification plan

Incisive Enterprise Verifier incorporates Desktop Manager, a subset of Incisive Enterprise Manager, to drive the verification process right from the planning stage. When combined with the guidelines in the planning and management component of the included Incisive Verification Kit, your team can automatically capture verification objectives from their written verification plan, create a vPlan executable specification, and

automatically compare progress against the vPlan. Furthermore, the combined results from formal analysis and dynamic simulation can be automatically backannotated and overlaid next to each other in the vPlan report to ensure all points of interest have been covered by at least one class of engine.

### Assertion-driven simulation

The same assertions used in formal analysis can be automatically reused by Incisive Enterprise Verifier to generate new dynamic simulation stimulus for the design. You can replay these automatically generated HDL tests—in effect, a “synthetic testbench”—to recreate the assertion or failure behavior using dynamic, simulation-based ABV.

### Cover point targeting

This capability is a unique application of Incisive Enterprise Verifier’s constraint solver and formal engines in combination with dynamic simulation. Users can select a cover point of interest, the formal engines figure out an optimal way to reach the selected state, and then Incisive Enterprise Verifier automatically creates and drives required stimulus back into the simulator. This speeds verification of designs faster than possible with the traditional application of trivial directed tests.

### Guide pointing

This capability uses formal analysis to hit deep states in the design not otherwise possible. Guide pointing allows you to specify intermediate states along the way to a deep state. It’s a classic “divide and conquer” approach to use your knowledge to break down the problem. Incisive Enterprise Verifier then uses formal analysis to hit these intermediate states (guide points) specified in sequence.

In effect, guide points are a sequence of covers, where the tool proves reachability to each guide point. As each guide point is hit, the design is initialized by simulation to this state to start exploration to hit the next guide point in the sequence. Once the final guide point is

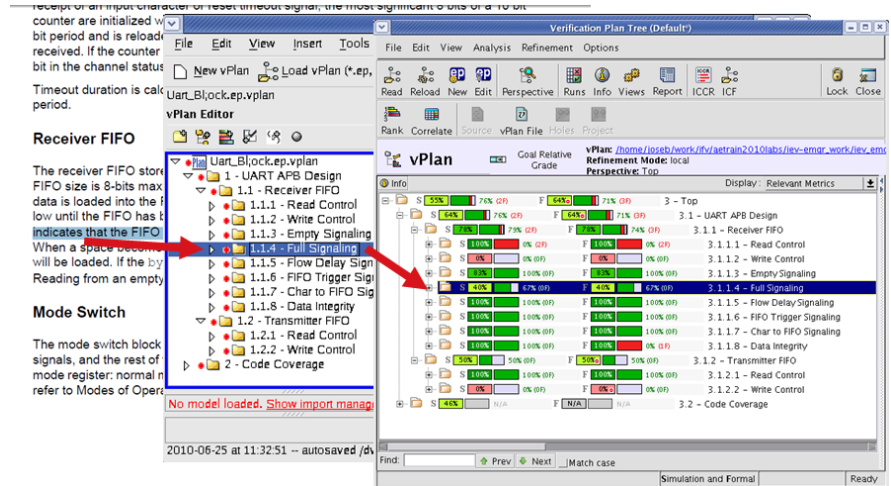


Figure 3: The Desktop Manager, included with Incisive Enterprise Verifier, can create an executable vPlan from your written specification; this plan drives all of your formal and dynamic simulations, with the coverage results from multiple runs automatically backannotated into the vPlan for a “total coverage” view

hit, Incisive Enterprise Verifier formally explores all the active assertions present in the environment.

### Search pointing

With search pointing, you can run a dynamic simulation to a point of interest and then apply the formal engines to explore the state space from that point in time. This process can be repeated to alternate runs of simulation and formal analysis. This enables verification of much larger designs/state spaces than possible with standalone formal methods.

### Automatic formal analysis

Incisive Enterprise Verifier’s automatic formal analysis capability automatically extracts from the design common assertions that can easily be overlooked or that are just plain tedious to write by hand. Either way, because the checks are automatically created, they are generated consistently across the entire RTL code base, and the correctness of the assertions is guaranteed. The bonus here is that no time will be required to debug these assertions themselves. Instead, you are free to focus solely on debugging failures or incorrect RTL behavior.

Anyone on a design or verification team can and should run automatic formal analysis on all designs in the same way you run code coverage in dynamic simulations; i.e., just turn it on and let the

machine do the work. It’s a simple and low-effort verification activity that can catch bugs “for free.”

### Leading-edge formal engines with smart automation

A combination of complementary, state-of-the-art formal engines from production-proven technologies and world-renowned researchers deliver the industry’s highest performance and capacity. To optimize formal analysis performance even further, built-in distributed processing allows you to leverage the broad engine assortment by running them in parallel for multi-fold performance gains.

### Broad assertion support and interoperability

Incisive Enterprise Verifier supports the same set of assertions as Incisive simulation, acceleration, and emulation tools. This includes assertions written in Property Specification Language (PSL), SystemVerilog Assertions (SVA), Open Verification Library (OVL), and the open source Incisive Assertion Library. Incisive Enterprise Simulator XL, the engine behind Incisive Enterprise Verifier’s dynamic simulation capabilities, supports all IEEE-standard languages.

### SimVision debug and analysis environment

An integrated GUI environment and Tcl interface provides you with an easy-to-adopt debug and analysis environment—the same as that in Incisive Enterprise Simulator XL, and similar to that of other simulators. The complete environment includes built-in linting, waveform viewing with source code linking, source code value annotation and tracing, structural analysis, vacuity and sanity checks, coverage reporting, and overall verification management. When Incisive Enterprise Verifier detects an assertion violation, it generates a counter-example waveform to aid debugging. Conversely, a “witness trace” waveform can be displayed to show an example of the assertion passing. You can also generate a simple testbench for use in an Incisive Enterprise Simulator XL dynamic simulation to validate the exposed functional bug or for regression runs. Together, these capabilities allow design teams to instantly deploy and use Incisive Enterprise Verifier in their production flows.

Throughout the design and verification flow, SimVision provides hardware analysis checks, source browsing, transaction and waveform viewing, and complete code/transaction/assertion/functional coverage analysis. APIs based on industry standards are available at all levels to enable user-defined checks and analysis. Bottom line: you only have to learn one debug environment.

#### Total coverage analysis

Incisive Enterprise Verifier supports “total coverage analysis,” including all coverage metrics commercially available—functional, HDL code, dynamic assertion coverage, and formal analysis results—which are all displayed together in one GUI and textual reporting system. This ensures that all functionality is fully tested, allowing you to achieve first-pass silicon success.

Leveraging functional and assertion coverage in particular, an executable functional test plan (the vPlan) measures the progress of verification, and functional analysis automatically identifies holes in the

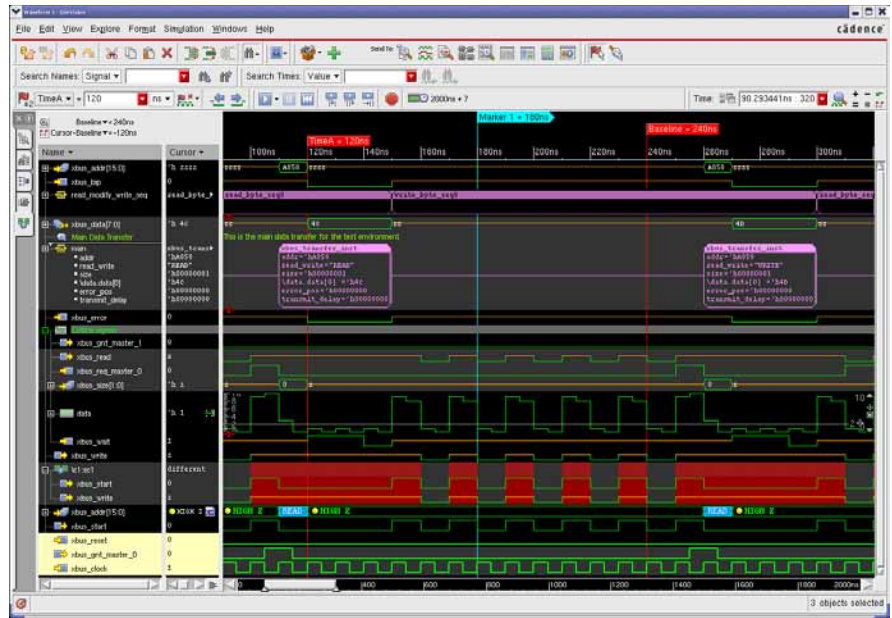


Figure 4: SimVision supports dynamic simulation signal-level and transaction-based flows across all IEEE-standard design, testbench, and assertion languages, in addition to concurrent visualization of the hardware, software, and analog domains

test coverage. Since functional coverage is a meaningful and direct measure of the completeness of your verification, this analysis increases the predictability of your verification schedule.

#### Multi-language, dynamic testbench simulation with Incisive Enterprise Simulator XL

Incisive Enterprise Verifier not only leverages Incisive Enterprise Simulator XL engines for its dual formal and dynamic simulation features, but all of the capabilities of XL are available to users.

The benefits of Incisive Enterprise Simulator XL include:

#### Increased predictability

- Drives your dynamic simulation process from plan to closure with the vPlan executable specification
- Applies coverage-driven verification and debugs complex hardware/software interactions and embedded software via Incisive Software Extensions

#### Higher performance

- Delivers the highest possible performance for mixed-language designs, across multiple levels of abstraction
- Enables “hot swap” of the software-based, dynamic simulation in/out of the Cadence Palladium® XP verification computing platform for additional performance

#### Enhanced productivity

- Reduces “time to first test” for verification novices and experts alike
- Speeds the construction, configuration, understanding, and usage of verification IP with the Incisive Verification Builder component
- Accelerates the setup, debug, and integration of verification environment components with 500+ HDL analysis checks that flag syntactic, semantic, and functional errors
- Automates generation, assertion checking, and functional and code coverage to provide a “total coverage” view

- Single-kernel architecture provides native, dynamic assertion support with PSL, SVA, and OVL, plus the Incisive Assertion Library, which allows users to insert common assertions into their designs quickly
- Reduces the time to discover and correct logic and transaction modeling errors via an integrated graphical debug environment

### Comprehensive standards support

- Supports all IEEE-standard languages and interfaces, enabling full legacy and third-party IP usage
- Supports the Si2 Common Power Format (CPF), an open specification language that captures all power-specific design intent

## Incisive Enterprise Simulator XL Feature Highlights

### Heterogeneous single-kernel architecture

The Incisive heterogeneous single-kernel architecture enables unified simulation through behavioral, transaction, register-transfer, and gate levels of abstraction. It uses a unique interleaved native-compiled architecture that supports all open and IEEE-standard languages including Verilog®, SystemVerilog, VHDL, *e*, SystemC®, the SystemC Verification (SCV) Library, CPF, PSL, SVA, OVL, and the Universal Verification Methodology (UVM) class library. Design and testbench models can be interleaved in any language and any level of abstraction without the performance and integration overhead caused by co-simulation.

### Rapid creation of libraries of reusable tests

Incisive Enterprise Verifier fully supports the testbench reuse component of the Universal Verification Methodology (UVM). The UVM describes how to create reusable verification components in any IEEE-standard language and provides guidelines for setting up multi-language interfaces to existing IP for maximum operational flexibility. Example UVM guidelines include recommendations for structuring classes, virtual interfaces, and packages for unrestricted portability.

### Constraint-driven stimulus generation

Using either the IEEE 1647 *e* language or IEEE 1800 SystemVerilog (or both together), Incisive Enterprise Simulator XL supports constraint-driven stimulus generation, which automates the process of generating functional verification tests. By specifying constraints, you can target the generator quickly and easily to create any test in your functional test plan.

You can even generate tests on-the-fly based on the current design state, making it possible to detect hard-to-reach corner cases.

When combined with the “sequence” feature of the UVM, stimuli that exercise corner-case scenarios at the block level can be reused at the system level to verify how the entire chip behaves in that corner case. All scenarios are written out into a reusable format, supporting the creation of portable libraries of protocol checkers and other structured behaviors for reuse on future projects, or system-level verification of the same project.

## Specifications

### Pure formal analysis design language support

- Verilog (IEEE 1364-1995, IEEE 1364-2001)
- SystemVerilog (IEEE 1800)
- VHDL (IEEE 1076-1987, IEEE 1076-1993)
- Mixed-language environments
  - Finite state machine (FSM) coding
  - Verilog, VHDL, and mixed-language support

### Pure formal results analysis

- Debug and GUI
  - Assertion manager
  - Waveform viewer
  - Source code browser
  - Source code value annotation
  - Driver and receiver tracing
  - Vacuity and sanity checks
  - Assertion triggering
- Reporting
  - Status and proof diameter reporting
  - Assertion coverage reporting
  - Formal coverage reporting
  - Cone-of-influence analysis

### Assertion support

- PSL and SVA (the IEEE-standard assertion languages)
- Open Verification Library (OVL)
- *e* testbench assertions
- Incisive Assertion Library (included)
- Common compile and elaboration mechanism with the Incisive platform
- Common user interface with the Incisive platform
- Dynamic assertion evaluation
  - Natively compiled with HDL for highest performance
  - Can be embedded in the HDL or in separate file(s)
  - Recorded as transactions for direct display in waveform window
  - PSL and SVA assertions treated as first-class simulation objects for easy debugging

### Dynamic simulation

- Single-kernel simulation engine
  - Verilog (IEEE 1364-1995 and IEEE 1364-2001 extensions)
  - SystemVerilog (IEEE 1800)
  - *e* (IEEE 1647)
  - VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 (VITAL 2000))
  - SystemC (IEEE 1666, OSCI® SystemC v2.2)
  - CPF
- Compile
  - Native compilation technology goes directly to host processor machine code, which maximizes performance
  - Intelligent incremental compile reduces compile times
- Capacity
  - Typical 10M gate equivalents in 32-bit OS (4GB addressable)
  - Typical 100M gate equivalents in 64-bit OS
- Server farm
  - Platform computing LSF
  - Oracle Grid Engine

## Simulation and mixed formal/simulation results analysis

- Debug and GUI
  - Waveform window
  - Register window
  - Unified transaction/signal viewing
  - Schematic tracer
  - Expression calculator
  - Signal flow browser
  - Source viewer
  - Error browser
  - Tcl/Tk scripting for customizable displays
  - Log signal and transaction data to SST database
- Performance analysis software outlines areas of code where most simulation time is spent
- Code coverage
  - Supports Verilog, SystemVerilog, VHDL, and mixed-language designs
  - Automatic FSM extraction
  - Coverage attributes supported include blocks, paths, expressions, variables, gates, FSM (states, sequences), and toggle
  - Coverage reuse
  - Rank order coverage contributions
  - Bit-wise expression scoring
- Functional coverage analysis
  - Supports Verilog, SystemVerilog, VHDL, e, SystemC, SCV, PSL, SVA, and OVL
  - Logs data to SST2 database
  - Tcl/Tk scripting for custom analysis

## HDL analysis

- 500+ checks to lint and analyze code for:
  - Synthesizability
  - Race conditions
  - Code reusability
  - Clock domain synchronization
  - FSM coding
  - Acceleration policy checks
- Gate-level netlist analysis for any DFT errors introduced during synthesis

- Verilog, SystemVerilog, VHDL, and mixed-language support
- Powerful customization capability using VPI/VHPI
- Graphical interface to sort, filter, and analyze messages with source code

## e testbench analysis

- 200+ checks to lint and analyze code for:
  - Code reusability as per Universal Verification Methodology (UVM) compliance rules
  - Performance analysis
  - Race conditions
  - Pre-defined coding style rules
  - Generation constraints
- Graphical interface to sort, filter, and analyze messages with source code

## Verification builder

- UI support for configuration of UVM-compliant Universal Verification Components (UVCs)
- Outputs UVCs in either e (IEEE 1647) or SystemVerilog (IEEE 1800)

## Cadence IP support

- Design IP
  - Functional Verification Kit for ARM® processor-based designs
- Verification IP (VIP)
  - Supports assertion-based VIP included in the Cadence VIP portfolio
  - Supports all simulation-based UVCs, transaction-based VIP, assertion-based VIP, and SpeedBridge® rate adapters used in emulation
  - Supports the full portfolio of Cadence UVCs\* and memory models

*\*Cadence UVCs include a comprehensive Compliance Management System that leverages vPlans to exhaustively verify protocol compliance.*

## Third-party support

- ASIC libraries
  - 30+ ASIC vendors have certified their libraries for the Incisive platform

- 150+ unique libraries
- Models
  - Third-party model support through the Cadence VIP partner program
- Software
  - Third-party software support through the Connections® program with 30+ verification company partners

## Interfaces

- Tcl command interface
- PLI (IEEE 1364)
- DPI (IEEE 1800)
- VPI (PLI 2.0, IEEE 1364)
- OMI (IEEE 1499)
- VHPI
- Compiled SDF
- VCD and SST2 interfaces

## Platforms

- Oracle Solaris
- Linux

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



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