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Faster Hardware Verification and Software Validation for Supercomputers

Fujitsu and Cadence

Courtesy of Fujitsu Ltd.

The Customer

Headquartered in Tokyo, Japan, Fujitsu is the leading Japanese information and communication technology (ICT) company offering a full range of technology products, solutions, and services. The organization's goal is to enable a "Human Centric Intelligent Society."

Fujitsu's high-performance computing systems provide the ability to address high-magnitude problems such as product, material, and new drug development, as well as scientific discovery. To meet the high-performance computing requirements, Fujitsu adopts higher speed I/Os and memory to get higher data throughput; smaller semiconductor process technology to pack more cores in; redundant logic and resilient cells to attain higher reliability; and features such as additional instruction sets, optimized cache structures, and interconnect packet processing hardware to reduce latency.

The Challenge

The hardware features that Fujitsu has adopted have achieved the required high performance. However, these features also inevitably result in the combinatorial explosion of parameters and scenarios during verification. In one instance, one 100,000-gate module of the system contained tens of thousands of combinations.

This combinatorial explosion is virtually impossible to handle. To address this challenge, Fujitsu applied a "divide and conquer approach". In order to narrow down the combinations, Fujitsu divided the entire system design into single modules. However, through this approach, each module requires accurate input constraints. "Having too many constraints results in under-verification and too few causes over-verification," noted Takahide Yoshikawa, senior researcher, Fujitsu Laboratories.

To develop ideal module constraints, the engineers need to understand the accurate module behavior within the entire system—a challenging proposition in such a huge and complicated system. "We determined that the most practical key to break down system behavior into module behavior would be to connect each module, including processor cores, and run processor-related testing software and real applications on these cores," said Yoshikawa.

The Solution

Their challenge led the Fujitsu team to a software-driven verification and emulation environment. To run the processor-related software, the team needed to run long simulations (tens of billions of cycles) on large system-wide models (tens of millions of gates). Obviously, PCs wouldn't be powerful enough. That's why Yoshikawa and his team turned to Cadence's Palladium XP verification computing platform, attracted by the solution's scalability to up to two billion gates, versatility, and ability to enable enhanced productivity (via performance up to 4MHz and support for up to 512 simultaneous users).

The team set up the CPUs and other I/O models on the Palladium XP platform. Since the emulator capacity is limited, some modules were replaced with a dummy module that is much smaller than the real one, but able to simulate the practical workloads. These dummy modules can cause fault

Key Challenges

- Achieve high performance of computing systems
- Accelerate verification of high-performance computing systems
- Better understand module behavior at the system level

Cadence Solution

- Palladium® XP verification computing platform

Lessons Learned

- Automatically generate assertions, via module level verification, to find overlooked behaviors

Results

- Caught 1/3 of system bugs
- More than 150% faster overall verification process and savings of more than one re-spin
- At least 300% faster post-silicon bring-up
- 600% better engineering productivity

injection, simulate analog delays, and interpret scenarios to cause complicated patterns like burst errors. Once overlooked behaviors are captured, these should be reproducible. To achieve this, the dummy modules are controlled by registers and then can be synchronized with testing software.

The Palladium XP platform provides assertion and code coverage. Assertions and coverages are shared by the module and the system levels. After running software, if new assertions are fired or new lines are covered, the overlooked behavior is caught and feedback is provided to fix the input constraints at the module level. Even though only some part of these behaviors can be caught by this software-driven verification environment, designers are alerted and can search any other problems through reviews. These newly found behaviors are fed back to the module-level verification environment, and allow hunting for other bugs.

The Fujitsu team also ran the operating system and practical applications on the entire system model in the Palladium XP platform. This helped them verify their peripheral and interconnect software drivers prior to tapeout. "The Palladium XP system helped us achieve 300% faster post-silicon bring up," noted Yoshikawa.

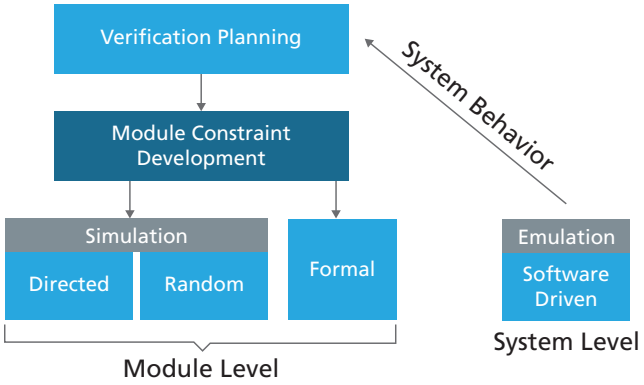

Figure 1: Software-driven verification environment to assess system behavior

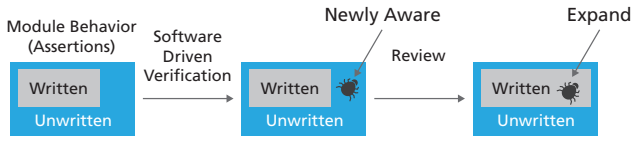

Figure 2: Finding overlooked behavior through the software-driven verification

The Results

By using the "divide-and-conquer" approach driven by the Palladium XP platform and software-driven verification, Yoshikawa and his team were able to catch one-third of the bugs in their system. These bugs were caused by overlooked behaviors that are detectable only at the system verification level. "If all module behaviors were completely written in assertions, these bugs would be captured at the module level," noted Yoshikawa. "Palladium XP plays a valuable role in helping us capture system bugs."

Using the Palladium XP platform also helped the team achieve 150% faster overall verification process and prevented more than one re-spin, along with 600% better productivity.

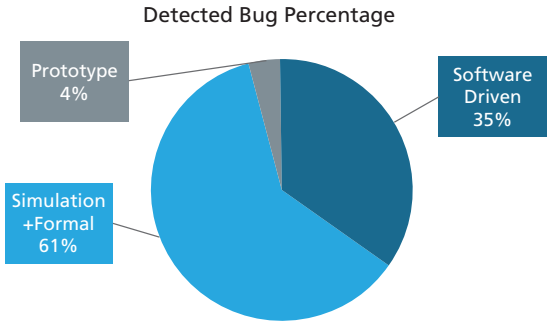

Figure 3: How Fujitsu detects system bugs

Lessons Learned

The team found that some behaviors were overlooked because of unwritten assertions. These overlooked behaviors are, however, sometimes critical because they can cause system errors. It's impractical for designers to write all the assertions for these, as they would be too many and be too complex to handle manually. So, Fujitsu needed a way to find these missing assertions.

In module-level verification, some tools can capture dynamic module behavior by running test scenarios and generating assertions automatically. These assertions show the designers the overlooked behaviors. In software-driven verification, running test programs is a way to capture dynamic system behavior and generate some metrics automatically. "This capability would be a desirable use model for system verification," noted Yoshikawa.

Summary

"High-performance computing systems will continue to grow larger and more complex," said Yoshikawa. "We will continue to rely on the Palladium XP emulation platform to capture overlooked behaviors."

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