

Cynthesizer Solution

The high-level synthesis leader

The Cadence® Forte Cynthesizer™ solution automatically creates high-quality RTL design implementations for ASIC, system-on-chip (SoC), and FPGA targets from a high-level SystemC/C++ description. The Cynthesizer solution's proven successes in hundreds of production designs around the world are testament to its consistently high quality of results, mature feature set, and complete design coverage.

Cynthesizer Overview

The Cynthesizer solution is the next generation of high-level synthesis technology. It is based on experience from more than a decade of production SystemC high-level synthesis deployment. With the Cynthesizer solution, design teams can quickly create high-quality RTL implementations from highly abstract SystemC models. The SystemC models can be easily created using the new Cynthesizer Workbench SystemC integrated development environment (IDE), retargeted to new technology platforms, and reused more easily than traditional hand-coded RTL. And, the Cynthesizer solution will allow designers to actively make tradeoffs to power in addition to area and performance from right within the high-level synthesis environment.

The Cynthesizer solution incorporates breakthrough synthesis technologies that combine the scheduling and allocation phases of the process to improve predictability and quality of results. New scheduling algorithms allow the Cynthesizer solution to quickly evaluate multiple design micro-architectures and schedules to find

the best possible area, performance, and power based on the designer's constraints.

Cynthesizer Low Power

With the Cynthesizer solution, design teams can automate complex low-power optimizations that are often difficult or impossible to realize

with hand-coded RTL. Designers can use the Cynthesizer solution's design exploration capabilities to trade off area, performance, and power for a given set of design constraints. Combined, these new optimizations can yield power reductions of 60% or more depending on the design.

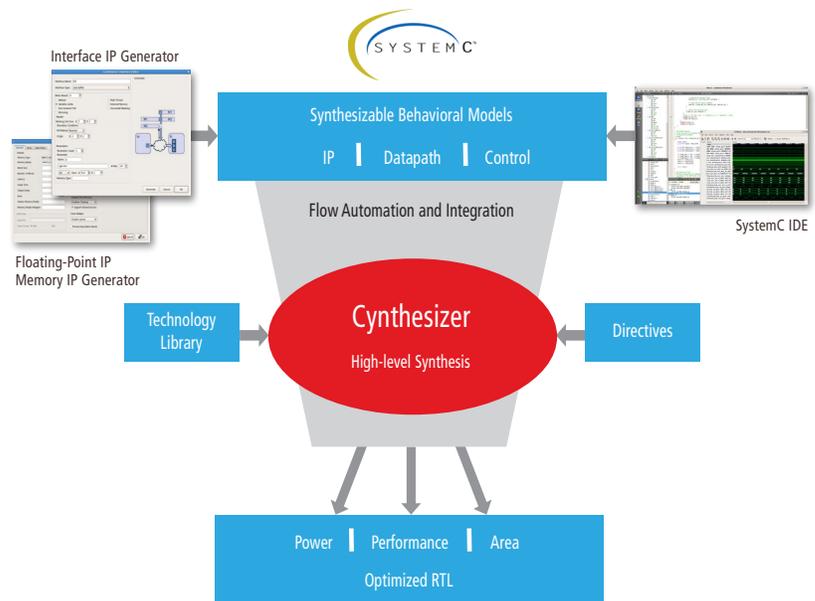


Figure 1: High-level synthesis with the Cynthesizer solution

Benefits and Features

World-class productivity and QoR

- Production-quality RTL
- Cutting-edge datapath optimization
- 2.0M gates/designer/year

Low-power design

- Clock gating optimizations during HLS
- FSM optimizations minimize mux select switching
- Memory optimizations tradeoff area and power
- Disables memories when not in use
- Clock-domain crossing circuitry
- 1/2- and 1/4-speed memory architectures
- RTL output coding style optimized for downstream RTL tools

Complete design support

- Datapath and control-dominated designs
- Most mature feature set
- Integrates with signoff RTL flow

High level of abstraction

- Compact coding style
- Untimed C++ behavior
- Explicit concurrency and structural models
- Built-in interface generator and IP
- Custom interfaces written in SystemC

Eliminate backend timing problems

- Exhaustively analyzes all timing paths
- Systematically produces RTL that meets timing

Increased return on engineering investment

- Easy retargeting
- Effective IP reuse
- Rapid design exploration

Early, accurate verification of complex designs

- Transaction- and pin-level simulation support
- Reusable testbench for SystemC and RTL

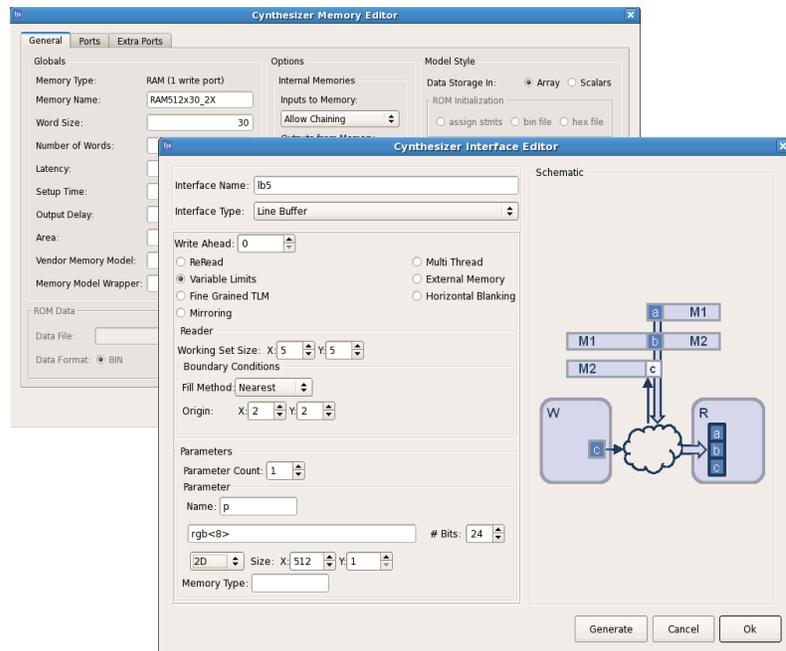


Figure 2: Cynthesizer Interface Generator

Cynthesizer Workbench

The Cynthesizer Workbench graphical user interface (GUI) incorporates a SystemC IDE, making SystemC development easy and intuitive for new users and advanced users alike. Beyond typical IDE features, the Cynthesizer Workbench makes it easy to quickly create new models using pre-defined design templates to reduce design and debug time.

The internals of the Cynthesizer Workbench have also been completely redesigned to allow faster design, debug, and analysis of SystemC models and the resulting RTL designs. The analysis environment includes SystemC and RTL source linking, a waveform view for simulation results, and other tools to optimize design results.

Datapath Optimization

The patented DpOpt technology can automatically identify optimization opportunities in the high-level SystemC design and synthesize optimized custom datapath components to meet the need. This allows designers to reduce circuit area and power and achieve circuit speeds unachievable through other means.

CynWare IP

The CynWare SystemC IP library and the CynWare Interface Generator™ give designers synthesizable building blocks to jumpstart their designs. Since these pre-designed elements are implemented in high-level SystemC code they can be re-targeted to different processes or QoR targets without performance or area penalties. The result is truly reusable design IP that accelerates the design and verification process.

The CynWare IP library contains high-speed simulation models and bit-accurate synthesizable models for all IP:

- Floating-point datatypes available in IEEE 754 single and double precision as well as other combinations of exponent and mantissa width defined by the user
- User-configurable connectivity interfaces such as line buffer, circular buffer, trigger-done, streaming data, FIFO-based, and memory interfaces.
- Clock domain crossing (CDC) circuitry for multi-clock designs
- Specialized communication interfaces, including frame buffers and bus interfaces for connections using the ARM® AMBA® AXI and AHB interconnects

Most Productive Path to Silicon

Traditional RTL design methods achieve approximately 200K verified gates per designer per year for new blocks. Cynthesizer users report results as high as 2.0 million verified gates/designer/year. These productivity gains are even more pronounced for designs where algorithms are changed or performance targets are modified. The Cynthesizer solution enables behavioral IP reuse, which dramatically reduces risk in your design schedules by completing tasks in hours or days that used to take weeks or months. These dramatic productivity gains can be achieved without compromising on performance, silicon area, or power. Cynthesizer users have demonstrated the ability to rapidly produce high-quality RTL for high-volume consumer products over more than ten years. They consistently achieve results equal to or better than hand-written RTL in silicon area and power consumption.

Increased Return on Engineering Investment

Semiconductor companies spend millions of dollars on design engineering and verification to produce production-worthy design source code. Unfortunately, with the traditional RTL design flow, the low-level cycle-by-cycle, explicit FSM nature of this source code means that you often have to create brand-new RTL even to make small modifications to the design. Using the Cynthesizer solution with high-level SystemC, your verified source code can be reused without modification for widely different process technologies

and clock speeds. Modifications to the algorithm, architecture, or interface can be made incrementally at a high level, where previously they required a complete rewrite of RTL. The Cynthesizer solution will significantly reduce your overall design effort and maximize your ROI.

Standards-Based SystemC Synthesis

The Cynthesizer solution supports industry-standard IEEE 1666 SystemC semantics. This standard allows designers to use familiar hierarchical decomposition techniques to manage design complexity. By supporting multiple threads, it allows design and verification of multiple algorithms operating concurrently, providing a level of accuracy not possible with other ESL languages. Because SystemC is a C++ library that adds hardware constructs, C or C++ algorithm code can be put into the context of a hardware module with hardware interfaces without any translation.

Eliminate Backend Timing Problems

The Cynthesizer solution ensures easy timing closure for the generated RTL by exhaustively analyzing each path and scheduling operations so they easily fit in the given clock period.

You begin the high-level synthesis process by specifying a target clock period and a technology library (foundry .lib file). The Cynthesizer solution uses patented datapath optimization technology to precisely determine the propagation delay

of each operation (such as an adder, multiplier, or multiplexer). Directives allow user control of how aggressively the Cynthesizer solution packs these operations into each clock period. Creating designs with the Cynthesizer solution can save months of backend effort by preventing timing closure problems.

Most Complete Design Flow

The Cynthesizer solution comes with a fully integrated automation system. One short TCL file can configure and automate all of the following:

- C++ compilation and linking
- Library, clock, and tool-directive settings
- SystemC simulation and RTL co-simulation
- Logic synthesis
- Formal equivalence checking between RTL and gates
- Power analysis
- RTL analysis and debug
- Design exploration for multiple configurations



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