Cadence Virtual System Platform for the Xilinx Zynq-7000 All Programmable SoC

An extensible virtual platform for faster embedded software development

The Cadence® Virtual System Platform for the Xilinx® Zynq-7000 All Programmable SoC provides an easily extensible virtual platform for embedded software development, long before the RTL is completed or the board is available. Using this virtual platform, the software team can work in parallel with the hardware team without needing access to physical hardware or to the RTL that will be instantiated in the Zynq's programmable fabric. With parallel work flows, early access to hardware, and superior visibility and control, the virtual platform enables concurrent delivery of hardware and software and reduces product development time.

Faster Embedded Software Development

A virtual platform is not just a replacement for hardware—it enables parallel development flows that are not otherwise possible. Virtual prototyping changes the way that embedded software is developed; first, by enabling software development in parallel with hardware development; and second, by providing full visibility and control of the software and hardware programming interface. With a virtual platform, it is now possible to develop and debug production-embedded software concurrently with the hardware design.

The Cadence Virtual System Platform's unified debug GUI provides fully synchronized, coherent multi-core hardware/software debugging. It comes with consistent breakpoints, single stepping, probing, tracing, and memory/register source-level debugging in either hardware or software models.

The Virtual System Platform runs the same binary that runs, or that will run, on the physical hardware—the visibility it provides into the instructions executed and the transactions between components is the same as what will be on the actual hardware.

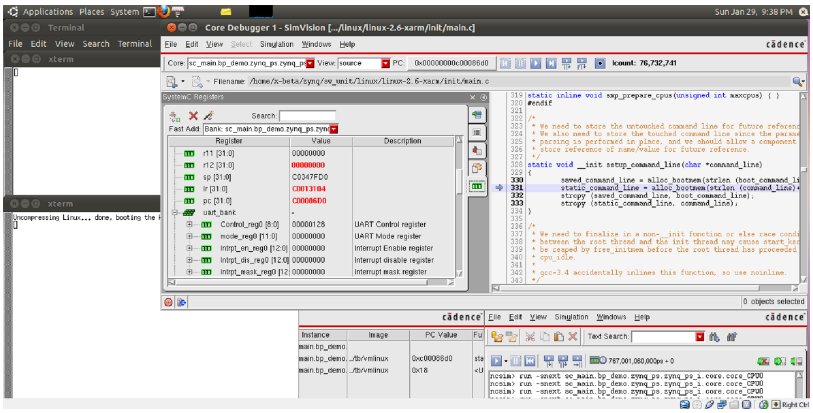

Figure 1: Screenshot of the virtual platform debug screen

Easy Extension with Transaction-Level Models

Developing high-performance virtual platforms has traditionally been difficult and time consuming. The Xilinx Zynq virtual platform comes with transaction-level models (TLMs) pre-defined for the processing system.

Unlike handwritten models that take a lot of effort, the Cadence Virtual System Platform Creator includes an automated code generation tool: "tlmgen." Tlmgen reads an IP-XACT or text descriptor file to produce a TLM 2.0 framework including embedded register intent awareness and register error checking, all without requiring any TLM 2.0 knowledge. These generated models include all read/write registers so that they can be used as is within the Zynq virtual platform. They can also be extended for detailed functionality.

This TLM-based approach requires much less time than the development of the RTL for those devices and accelerators within the FPGA.

Now, software development can begin months prior to RTL implementation and verification.

Benefits

- Quickly develop and deliver production-ready software for a standard or extended Zynq-7000 All Programmable SoC
- Eliminate hardware/software development dependencies
- Begin software development before firmware, board hardware, and RTL are available
- Start earlier and work faster with full hardware/software visibility and control
- Customize the Zynq-7000 All Programmable SoC in just days by using high-level models
- Create a feedback loop between hardware and software developers

Additional Features

Deploy virtual platforms for software development

Customized virtual platforms that have been created by extending the off-the-shelf Zynq-7000 All Programmable SoC can be packaged and exported for easy delivery to the entire software development team. The exported virtual platform interfaces with the Xilinx Eclipse Software Development Kit (SDK) to provide a complete and easy-to-use software development and debug environment.

Connect to the implementation flow

The use of fast functional models enables early and binary-compatible software development. However, it may be necessary to verify behavior for portions of the system by connecting cycle-accurate RTL models to the functional virtual platform. Cadence supports such development needs with its single SystemC™/RTL simulation engine and debugger.

Functional verification automation can be applied to the virtual platform with embedded software, improving overall system quality by exploring corner-case system conditions often only discovered after RTL is used to build the system. When run within a virtual platform, such verification can test responses to both software and hardware faults.

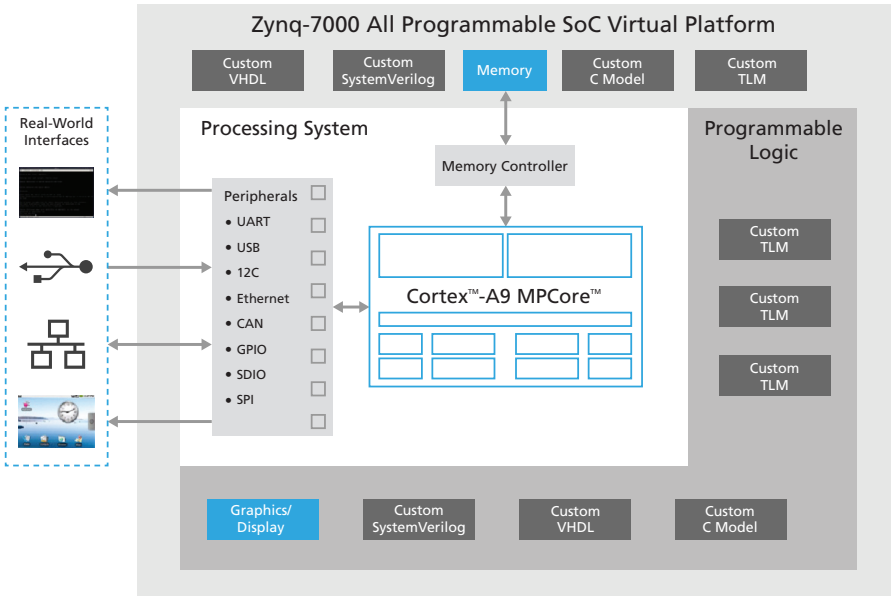

Figure 2: Overview of the Xilinx Zynq-7000 All Programmable SoC

Requirements

- System creation
  - Linux workstation, laptop, or virtual machine
  - 64-bit Red Hat Enterprise or SUSE Enterprise
  - 4GB of RAM minimum, 8GB preferred
- Software development
  - Linux workstation (32-bit or 64-bit; Red Hat or SUSE)
  - 2GB of RAM

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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