Cadence Accelerated Verification IP for PCI Express

Industry-leading validation solution with extensive track record of customer success

Cadence provides mature, high-performance Accelerated Verification IP (AVIP) for the PCI Express® protocol. Cadence® AVIP for PCI Express supports C++, SystemC, and UVM SystemVerilog user interfaces. Using Cadence AVIP, you can accelerate IP, subsystem, system-on-chip (SoC), and system-level validation to ensure high product quality while also achieving high engineering productivity.

Cadence AVIP for PCI Express

Cadence has established a proven track record in high-quality verification IP (VIP), including our extensive Verification IP Catalog and SpeedBridge® adapters portfolio. We've now extended our leadership with high-performance AVIP on the Cadence Palladium® XP Verification Computing Platform. To deliver high-end verification and validation performance, Cadence AVIP for PCI Express takes full advantage of the Palladium XP architecture by enabling you to achieve speeds that are hundreds of times greater than with simulation.

With support for C++, SystemC, and UVM SystemVerilog user interfaces, you can meet a variety of accelerated validation challenges, while only having to learn a single AVIP.

Benefits and Features

- Complies with the PCI Express protocol specifications versions 1.1, 2.0, and 3.0
- High performance: C/C++/SystemC™ interface commonly enables performance gains of 200-500x relative to SystemC software-only simulation
- Supports configurability as either root complex, end point, or both
- Supports both PIPE and serial interfaces for connection to your design
- Supports 8-bit, 16-bit, 32-bit, and 64-bit bit PIPE data widths
- Supports all types of posted and non-posted transaction level packets (TLPs)
- Rich user APIs to develop or integrate with user testbenches
- Configuration "knobs" allow you to make tradeoffs between verification functionality and performance. Functionality such as transactions trace, data log dumps, checking, and coverage for UVM environments are under user control and can be traded for higher performance

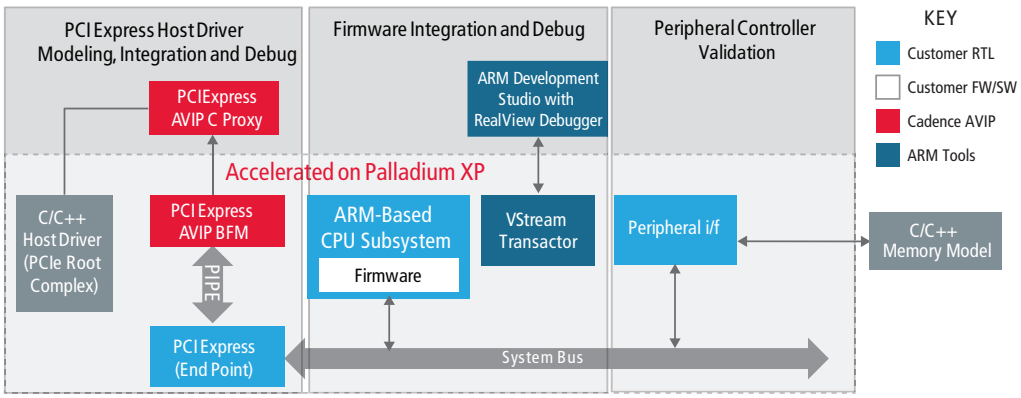

Figure 1. Typical firmware/driver/software integration environment using AVIP for PCI Express

Achieve highest performance when using C/C++/SystemC testbenches

- C++/SystemC interface enables performance gains of 500x relative to SystemC software-only simulation
- Enables software integration and validation at subsystem and SoC levels. Stimulus drivers can be integrated using the rich C/C++/SystemC API of the AVIP. A stimulus driver can reside either on the Palladium XP Linux-based simulation-acceleration host or on an external, non-native Linux host.

"As Cadence promised, our validation environment now runs hundreds of times faster than with simulation. Accelerated VIP running on the Palladium XP increased my team's productivity by 100%."

Tony Gladvin George
Verification Engineer,
Samsung

Enables reuse of UVM simulation environments

- UVM SystemVerilog interface enables existing simulation environments to be reused at higher performance with key simulation-based verification capabilities, typically used for RTL verification
- UVM SystemVerilog interface typically enables performance gains of 25-100x or more relative to UVM software simulation

The Cadence AVIP architecture is uniquely designed to enable a variety of RTL verification and software integration and validation goals. Cadence AVIP provides a variety of user interfaces, allowing you to apply a single AVIP to each of these verification/validation challenges.

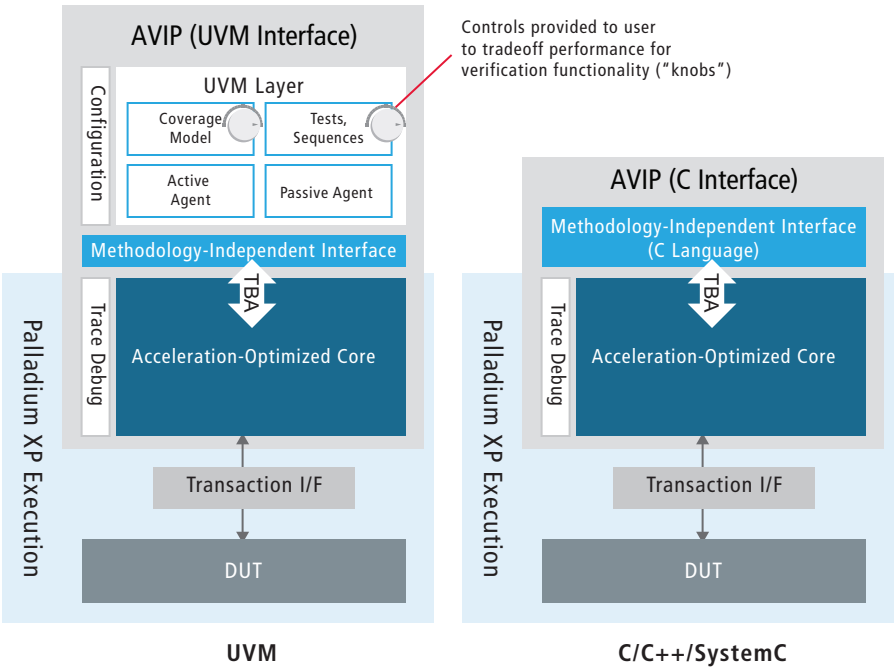

Figure 2: AVIP for PCI Express architecture diagrams showing UVM and C/C++/SystemC interface options

Transaction Size (TLP Data Words)	Performance Gain Relative to Simulation*	
	Memory Read Transactions	Memory Write Transactions
128	318X	391X
512	390X	400X
1024	408X	406X

Table 1: AVIP for PCI Express 2.0 transaction time speedup over simulation using C/C++/SystemC interface

* 80% of time spent in Palladium environment, 20% in testbench; design size >5Mgate

Deliverables

- AVIP for PCI Express software
- User Guide
- Examples for all available user interfaces

Cadence Services and Support

- More information regarding the Cadence VIP Catalog is available at: http://www.cadence.com/products/fv/verification_ip
- Hands-on demos of the Cadence simulation Verification IP are available at the Xuropa online community: www.xuropa.com/cadence
- Cadence application engineers can answer your technical questions by telephone, email, or Internet; they can also provide technical assistance and custom training

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**