System-Level Electro-Thermal Analysis of $R_{DS(ON)}$ for Power MOSFET

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Abstract

A coupled-electro-thermal $R_{DS(ON)}$ (drain to source ON resistance) co-analysis methodology for Power MOSFET is proposed. The methodology contains two functional modules: 1) physical field solvers and 2) equivalent circuit/network solver. The field solver resolves the electrical and thermal field variables by the conventional 3D finite-element method, while the network solver can achieve accurate and efficient results by connecting the equivalent electrical, thermal and flow circuits that are extracted from the system through advanced numerical computational schemes. The integrated equivalent network can then be solved by a generic circuit solver for steady state and transient responses. The methodology is demonstrated, via simulation and measurement, on a 2.5MHz DCDC buck-boost converter. Good correlation between co-analysis methodology and laboratory measurements is achieved.

Keywords

$R_{DS(ON)}$, Electro-Thermal, and Power MOSFET

1. Introduction

For MOSFET, $R_{DS(ON)}$ is the total resistance between the drain and the source during the ON state. $R_{DS(ON)}$ depends on the junction temperature and gate-source voltage (V_{GS}). The power loss in any MOSFET is a combination of the conduction and switching losses. The conduction loss is defined as the product of [$I_{OUT}2$ x $R_{DS(ON)}$] of the MOSFET and its duty cycle, (V_{OUT}/V_{IN}).

$$P_{COND} = I_{OUT}2 \bullet R_{RDS(ON)} \bullet V_{OUT}/V_{IN} \qquad (1)$$

As shown in equation (1), the practical approach to reduce conduction loss is to minimize the total resistance, $R_{DS(ON)}$. Typically, the primary components of $R_{DS(ON)}$ for Power MOSFET include the channel, JFET (accumulation layer), drift region, and electrical parasitics (viz. die metallization, package wire bond, and PCB interconnect) [1]. Recent advances in silicon MOSFET technology have dramatically reduced the silicon resistance contribution to total resistance [2-3]. The resistance reduction is achieved by silicon area reduction. While this area reduction is desired, as it reduces product cost, this in turns impact the power/area (i.e. the power density). The increase in power density leads to higher local temperatures (hot spots) since temperature is proportional to power and volume, which is proportional to area. This effect could lead to technical situations that match the electrical requirements but local temperatures at the hot spots run risk to exceed max allowed temperatures for a process leading to reliability degradation. In turn the increased temperature has negative effect on mobility of carriers and thus reduces the desired electrical performance.

To analyze this feedback effect of temperature to electrical performance and gain information on the maximum temperature of the hot spots, the temperature effects of the three dimensional package and PCB contributions should be fully comprehend – particularly the non-uniform temperature distribution on the ON resistance extraction at system-level [4]. Many approaches have been developed to account for electrical performance impact due to steady-state and transient thermal effects on power MOSFET conduction loss [5-6]. While effective, these approaches solve the electrical and thermal physical mechanisms in stages (i.e. uncoupled). In this paper we present and discuss a coupled approach that can be used to assess and compute the impact of temperature rise, due to power dissipation of the die, on the resistance of the system (viz. silicon + package + PCB). A major advantage of the coupled electrical and thermal co-analysis approach is that the two physical mechanisms are solved 'simultaneously', as they happen in reality. The interaction and mutual influence between temperature variation and electrical parameters within the device should not be modelled in stages, or separately. Here we take the direct and essential approach to tackle the coupled electro-thermal problem. In Section 2 the coupled electro-thermal methodology, via the two functional modules, is detailed. Section 3 describes the DCDC buck-boost converter system device under investigation. Observations on the methodology and the comparative assessment with laboratory measurements are discussed in Section 4.

2. Coupled Electro-Thermal Co-Analysis Flow

As discussed above, the current (and hence the dissipated power) is a function of device temperature, which in turn, is determined by the dissipated power. Therefore the determination of device current (i.e. power) and a temperature represents a coupled electro-thermal problem. The co-analysis methodology contains two functional modules: 1) physical field solvers and 2) equivalent circuit/network solver. The field solvers resolves the electrical and thermal field variables by the conventional 3D finite-element method, while the network solver can achieve accurate and efficient results by connecting the equivalent electrical, thermal and flow circuits that are extracted from the system through advanced numerical schemes including Finite-Element Analysis (FEA) and Computational Fluid Dynamics (CFD). The integrated equivalent network can then be solved by a generic circuit solver for the transient and steady-state responses due to electrical and thermal interaction, and the heat dissipation to

the surrounding fluid is also taken into account. Figure 1.0 below shows the electro-thermal co-analysis process flow.

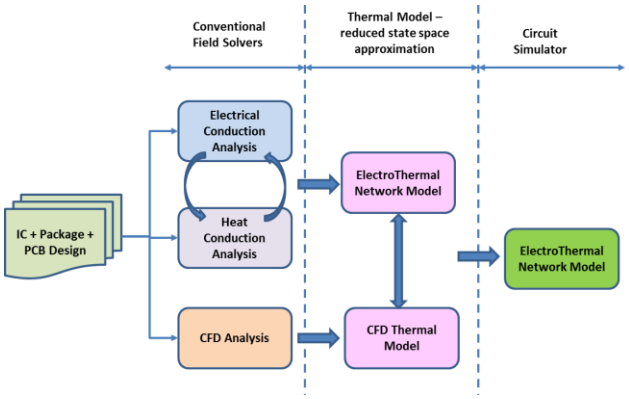

Figure 1: Electro-Thermal co-analysis flow.

2.1 Conventional Field Solvers

In the physical conventional field solvers the governing equations are solved iteratively based on the physics of electrical and thermal formulations respectively. For electrical [7] and thermal [8] solutions, the following equations are solved respectively:

$$\vec{J} = \overline{\overline{\sigma}} \cdot \vec{E} \qquad (2)$$

$$\overline{\overline{\sigma}} = f(T) \qquad (3)$$

$$\vec{J} \cdot \vec{E} = \frac{J^2}{\sigma} \qquad (4)$$

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) + Q = \rho c \frac{\partial T}{\partial t} \qquad (5)$$

Equation (2) is Ohm's law in point form, where J is a vector representing the current density, σ is a second order tensor with 9 components in general representing electrical conductivity, and E is a vector representing electrical field. The electrical conductivity tensor is a function of temperature as shown in equation (3). The Joule heating (power per unit volume) due to electrical current is expressed in equation (4). The thermal transport equation is given in equation (5), where T, k, ρ, c, Q indicate temperature, thermal conductivity, density, specific heat, and heat source respectively. Note that the thermal conductivity may have different values per the major geometrical axes.

The finite element analysis (FEA) adopted in the present study has been used in numerical simulation of multi-physics problems for decades, especially for the objects with complex geometrical configurations [9]. The essence of FEA, and of most other numerical methods, is to discretize the computational domain into small elements so the governing equations of physics can be solved efficiently and accurately within those elements [10]. To effectively carry out electrothermal co-simulation, the boundary conditions to be imposed to the problem are critical to achieve results that are coherent with physics and fit for realistic applications. Electrical boundary conditions should include the driving forces of electrical potential and the current requirements on the package and die to perform the functions as designed. These electrical boundary conditions are applied at specific ports or terminals in the geometrical model. Thermal boundary conditions are basically characterized as heat-in and heat-out mechanisms associated with the system. In general, the heat-in mechanism is the power input (or consumption) through the chip, and the heat-out mechanisms account for heat dissipation out of the system, including conduction, convection, and radiation [7]. Basically three different heat sources can be included in the present simulation: 1) component heating, 2) Joule heating, and 3) leak current heating. The component heating results from the dynamic switching of current in the chip, which is the main power consumption of the component. Joule heating is inevitable and well-understood when electrical currents flow through conductive paths with electrical resistance. The leak current heating could play a significant role in the advanced chip design because essentially the leak current increases with temperature, which then would cause the chip gets even hotter and may lead to failure if not carefully assessed. In the co-analysis discussed here, the extra power introduced by leak current will be calculated by iteration, according to a user-specified correlation between temperature and leak current power. Depending on the nature of problem of interest, different heat dissipation conditions may be applied at relevant surfaces or bodies where heat would transfer out of the system and to the environment [11-12]. By coupling the FETs power dissipation (static/transient) switching profile to the rest of the system (i.e. package and PCB), the impact of temperature rise can be computed using the electro-thermal methodology develop here. Figure 2 shows an example of a typical temperature distribution of an assembly of multiple packages on a PCB, where the mesh of the whole assembly is omitted for clarity, based on the conventional coupled electro-thermal analysis. Once the electrothermal analysis is done, a thermal network model is derived based on reduced state-space approximations.

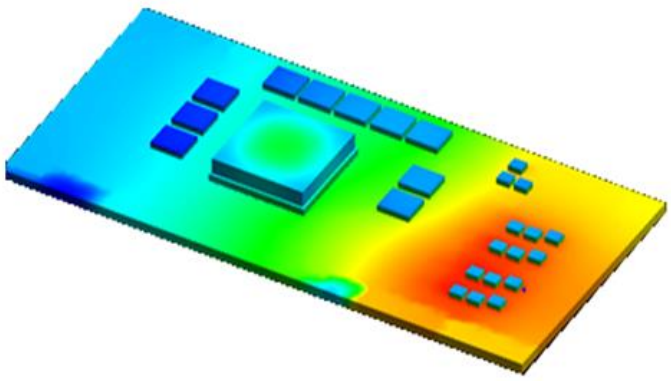

Figure 2: Example temperature distribution for a PCB solved using electro-thermal co-analysis methodology.

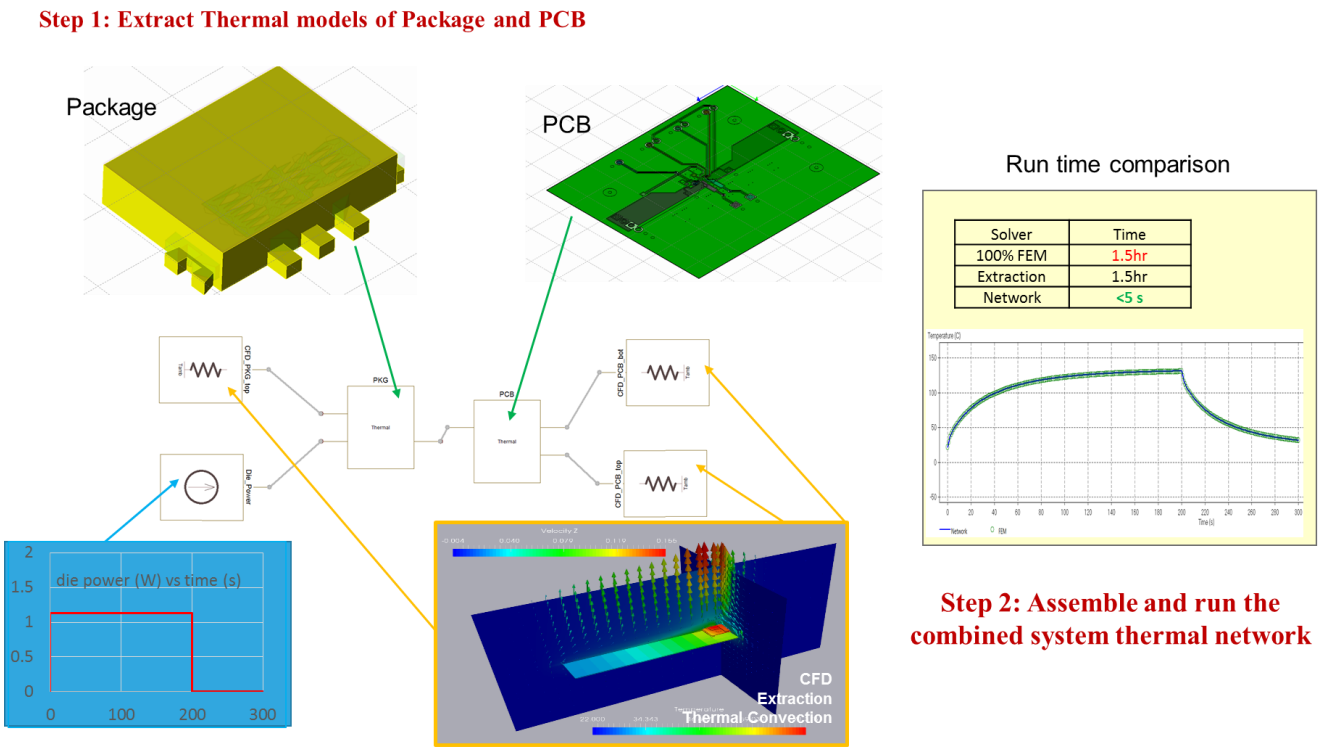

Figure 4: An example showing a package and PCB analyzed using the thermal network approach – significant decrease in computation/analysis time when compare to numerical computational and extraction techniques.

2.2 Equivalent Circuit/Network Solver

Three types of equivalent circuits can be extracted from the system by various methods: 1) electrical circuits, 2) thermal circuit, and 3) flow circuits. The electrical equivalent circuit extraction has been a mature technology for decades even for a complicated electrical system. For the thermal equivalent circuits, an advanced numerical scheme based on the finite-element method is employed to extract the essential parameters from the solid components.

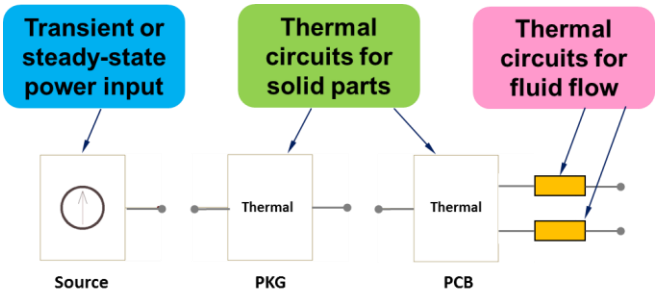

Figure 3: High-level connectivity of thermal network showing each component in the system and power input source/stimulus.

Furthermore, to include the heat transfer to or from the environment surrounding the solid components, the third type of flow circuits was created using the Computational Fluid Dynamics (CFD) technique. The technical details of the thermal network circuit formulations employed here are fully covered in references [13-15]. Figure 3 shows the high-level connectivity of the thermal network and Figure 4 shows an example of the thermal network methodology performed at the system-level (die + Package + PCB). Taking advantage of a generic circuit solver, both the transient and static responses of the system can be obtain in an efficient and accurate way, at any particular locations within the system specified in simulation.

3. DCDC System Description

The DCDC device under investigation is a dual-mode buck-boost 2.5MHz switching converter with seamless transition between buck and boost mode.

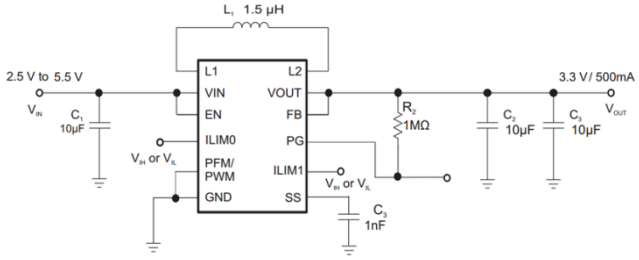

Figure 5: Simplified schematic of DCDC converter.

Continuous output current of 1A in buck mode with fixed and adjustable voltage versions. The converter is based on a fixed frequency PWM controller. For low load currents it supports PFM/PSM mode for improve efficiency over the

load current range. Figure 5 above shows a simplified schematic of the converter and external and external passives required. The HotRodTM Quad Flatpack No-Leads (QFN) are leadless packages specifically designed for power MOSFET applications [16]. They have small footprint, low self parasitics, and ideal for high current applications as shown in Figure 6 below. The electrical connections are made via lands on the bottom side of the component to the surface of the connecting substrate PCB/EVM.

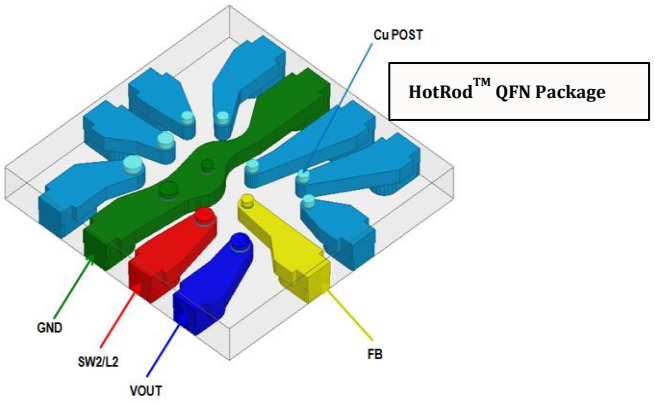

Figure 6: HotRodTM Package for Power MOSFET.

The FLIR (forward looking infrared) camera was employed to perform the thermal measurements on the EVM (evaluation module) PCB as shown in Figure 7 below under steady state power dissipation condition at room temperature 25°C.

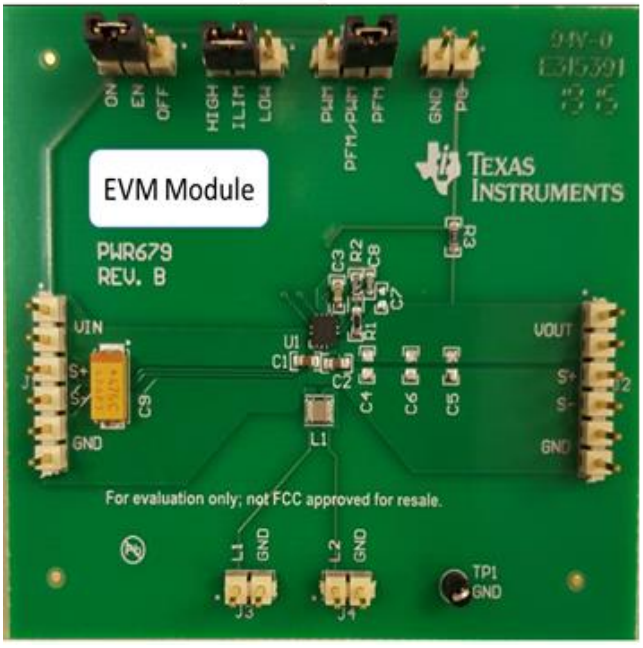

Figure 7: EVM module used to perform FLIR.

4. Observations and Concluding Remarks

As discussed above, the co-simulation methodology, developed in Section 2, was verified on a 2.5MHz DCDC system buck-boost converter under steady state power dissipation condition. This is when VIN is at the lower spec limit and VOUT is at the upper spec limit driving the maximum output current. Under this condition, the High Side FET of the BUCK stage is constantly and fully turned on with I_{IN} as shown in equation 6.

$$I_{IN} = (V_{OUT} \bullet I_{OUT}) \,/\, (\eta \bullet V_{IN}) \qquad (6)$$

With $V_{IN} << V_{OUT}$, $I_{IN} >> I_{OUT}$ resulting in maximum power dissipation at BUCK High Side FET. The BOOST stage FETs are switching with maximum duty cycle reducing efficiency, η, to conversion losses cause by-charging and discharging of FET gate capacitances as depicted in equation 7 – where C is capacitance, V_{GS}^2 is the gate-source voltage, and F is the frequency respectively.

$$P_{SWITCHLOSS} = \tfrac{1}{2} \bullet C_{GATE} \bullet V_{GS}^{\ 2} \bullet F \qquad (7)$$

The preliminary correlation between measurement (126.9°C, see Figure 8a) and simulation (135.9°C, see Figure 8b) appear to be fairly close. The observed difference can be further reduced by taking into account many variables - namely IR transparency of materials involved, emissivity of target surfaces, presence of air-flow in the measurement, and manufacturing process variations of the package and PCB. Differences of simulation versus measurement are also related to measurement tolerance, more complex arrangement of the real PCB including external passive components that partly emit additional heat due to joule heating but also partly help dissipating thermal power due to increased surface.

Additionally, the power loss for IR drop, including electrothermal impact was approximately 20% (0.1294W as compared to 0.108W at 25 °C). The power loss for package only, with and without thermal impact, was approximately (13% - 0.05617W vs 0.04952W at 25 °C) respectively. It is evident that for an accurate computation of conduction power loss, the temperature impact on $R_{DS(ON)}$ needs to be accounted for to assess realistic performance of power FET.

Further improvement of match between simulation and measurement might be possible and academically interesting. However, technically this is of little interest since the final customer application board might differ to an extent exceeding this simulation versus measurement difference by far. The analysis results, as they are now, are sufficient to determine during development of a DIE package combination if additional heat dissipating measures need to be deployed in the package, the DIE/FET size needs to be increased or the thermal connection to the board needs to be improved. Once those aspects are optimized, it would further indicate whether or not cooling would be required to the system (heat slugs, airflow, else) or the device depending on the use case of the

customer and the max ambient temperature in the customers application.

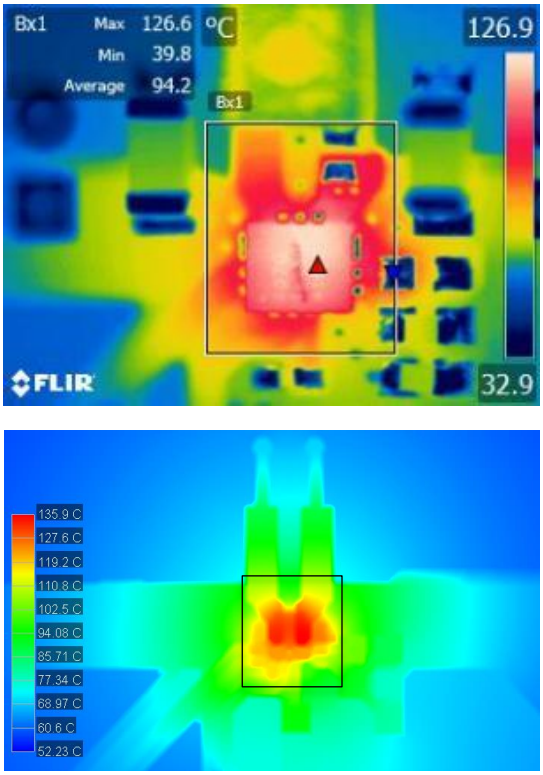

Figure 8: (a) Measured FLIR at room temperature and (b) corresponding system-level co-analysis via simulation as per developed methodology.

Since the time constant of the thermal development are magnitudes above the electrical switching frequency of a switch mode converter, the DC consumption of current in the electrical worst case operating point can be taken as a constraint to the thermal analysis. The thermal development in time and the thermal gradient can give further information on best placement of e.g. thermal shutdown circuits and maximum time to operate a device in this worst case operating point at the maximum ambient temperature. Alternatively the maximum ambient temperature can be determined for infinite operation under this worst case condition as well. We have demonstrated here an electro-thermal co-simulation methodology that takes into account the whole system (Silicon + Package + PCB) and assess impact of thermal effects on resistance increase. We have also shown that system-level thermal analysis can be very time efficient if the appropriate thermal network formulation is employed. We are currently working on refining the methodology to account for flow equivalent thermal model in the system-level combined electrothermal analysis.

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