Cadence’s Clarity:  
“I Can See Clearly Now” 

by Clive “Max” Maxfield
Do you recall the song “I Can See Clearly Now”? This catchy tune was first released by Johnny Nash in 1972, which was three years before I started my BSc in Control Engineering at Sheffield Hallam University, Yorkshire, England.

I’m humming the melody and thinking of the lyrics as I pen these words, except that I’ve just been looking at the Clarity 3D Transient Solver from Cadence, so the lyrics I’m hearing in my head are:

I can see clearly now the EMI is gone
I can see all EMC obstacles in my way
Here is that rainbow I’ve been praying for
It’s gonna be a bright (bright)
bright (bright) sunshiny day.

The reason for my current mellowness is that, with extreme performance coupled with virtually unlimited capacity and scalability, the Clarity 3D Transient Solver opens the doors to previously unobtainable levels of system-level electromagnetic (EM) simulation for use in electromagnetic interference (EMI) and electromagnetic compatibility (EMC) analysis. When we use the word “system” in this context, we are talking about the ability to perform EM simulation at the chip, package, circuit board (including rigid boards, flex, and rigid flex), module, and multi-board/multi-module assemblies including connectors and cables. Phew!

EMI and EMC
Now, it’s easy to get confused here, so let’s briefly remind ourselves that EMI—which may also be referred to as radio-frequency interference (RFI) when in the radio frequency spectrum—is a disturbance generated by an external source that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction. Although sources of EMI can be environmental (e.g., electrical storms and solar radiation), they are more commonly caused by other electrical systems or electronic devices.

By comparison, EMC refers to the ability of electrical equipment and systems to function acceptably in their electromagnetic environment, whatever that may be. That is, the goal of EMC is the correct operation of different equipment in a common electromagnetic environment. This is achieved by limiting the unintentional generation, propagation, and reception of electromagnetic energy, which may result in EMI or even in physical damage if the EM source is of sufficient intensity.

The Way We Were
Just thinking of Clarity’s cornucopia of capabilities is causing me to have flashbacks to the way we used to do things in circa 1980 when I was starting my career. My first position was at International Computers Limited (ICL) as a member of a team designing central processing units (CPUs) for mainframe computers. And my first task was to design an ASIC, which was to be implemented at the 5-micron process node. My digital logic design was performed at the gate- and register-level of abstraction using pencil and paper. Logic optimization was performed by another member of the team who was better at doing this that the rest of us. Functional validation was performed by all the members of the team looking at your schematics and asking pointed questions while you explained your logic and defended your decisions. Timing analysis was performed by you identifying any critical paths by eye and intuition, and then adding the gate delays and calculating the track delays by hand (no one I knew at that time could afford the state-of-the-art 4-function electronic calculators).

I have no idea who performed the layout of the ASIC—that task was undertaken by another team—although I did hear that they also accomplished their tasks by hand. When the finished layout was presented to me, it was in the form of a ginormous
ASCII text file, where ‘1’ characters indicated metal layer 1, ‘2’ characters indicated metal layer 2, ‘X’ characters indicated a via between metal layers 1 and 2, and so forth. Layout versus schematic (LVS) verification was performed by my printing this ASCII text file out in the form of around 20 strips each 20-feet long and 18-inches wide, using many rolls of sticky tape to form a gigantic rectangle in a large room that was reserved for this purpose, and then walking around (sans shoes) using colored crayons to mark off gates and tracks on my schematics and the corresponding transistors (silicon areas) and interconnect on the layout diagram.

One’s hope was to end up with everything in the schematic and layout colored appropriately; one’s fear was to discover discrepancies, or missing portions in the layout, or, as happened on occasion, to end up with unmarked areas in the layout that didn’t correspond to anything in the schematic, which resulted in some gnashing of teeth and rending of garb, let me tell you!

I also have no idea who designed the chip packaging including assigning pins to signals. Once LVS had been performed and everything had been signed off, with managers literally writing their monikers on the “ready for packaging” release, I didn’t hear or see anything until the packaged devices appeared several weeks later. Meanwhile, the PCB team had been performing their magic, which means someone must have told them what the pin assignments were going to be.

I didn’t become involved in PCB layout myself until a couple of years later when I was working for a small startup called Cirrus Designs. We had a mega-expensive system whose name I no longer remember, but it involved a large digitizing desk and mouse along with two large (for the time) monitors: one black-and-white where you issued command-line text-based instructions like “Place a pad at X=xxx and Y=yyy” and the other in color where you saw the results. The whole thing was powered by a fridge-sized computer. It was horrible. The best thing that happened to this system was when it overheated and caught fire, but that’s a story for another day!

When it came to things like EMI and EMC, as far as I know there were no simulation and analysis tools up to the task (we were more than happy if our deskside computers were powerful enough to run a screen editor). Apart from simply “winging it,” the only option available to us in those days was to build a physical prototype of the full system, send it out to a specialist company that had an anechoic chamber (also known as an EMC chamber) for EMI and EMC testing, and await the results in dread anticipation. In addition to costing lots of money, this could take weeks before we saw any results. If anything failed, and something almost invariably did, it was back to the drawing board. Thinking back, it’s amazing we actually managed to get any products out of the door.

Confiscating Chaos and Confusion

As radio commentator, motivational speaker, and author Steve Maraboli famously said in his book *Life, The Truth, and Being Free*, “It’s a lack of clarity that creates chaos and frustration.” Even though this book was published 11 years ago at the time of this writing, it’s as though Steve was peering into the future and channeling how Cadence’s Clarity 3D Transient Solver can confiscate chaos, confusion, and frustration, thereby making developer’s lives happier, easier, and more productive.

Cadence has state-of-the-art design and analysis tools for every portion of the design flow—chip design, package design, and board/module design. What is less well known is that, for the past few years, Cadence has been ramping up its capabilities in system-level simulation, analysis, and verification space (where no one can hear you scream) with tools like the Clarity 3D Transient Solver. In addition to performing EM simulation for EMI and EMC analysis and verification on chips, packages, and boards, the Clarity 3D Transient Solver means that it’s now possible to perform such simulations on full systems comprising multiple boards/modules, connectors, cables, and enclosures.

Let’s take a step back and think about this a bit. As we previously discussed, the traditional way of performing EMI/EMC verification involves building a physical prototype of the system and testing it in an anechoic chamber. It comes as no surprise to learn that it is horrendously expensive in terms of development time, resources, money, and time-to-market to build physical prototypes, test them, find problems, attempt to fix those problems, and
then perform the whole cycle over and over again. It’s obviously a much better solution to perform EM simulation to detect, identify, and resolve problems early in the design cycle, only building a physical prototype and performing real-world testing a single time at the end of the development process. The problem, of course, is finding an EM simulator that has the capacity and performance to simulate the full system, otherwise you have to partition things into smaller and smaller pieces, in which case you know only how these pieces work in isolation.

One underlying problem is that many of today’s software analysis tools were conceived and developed in the era of single core computing, which means they simply don’t scale well, even if they are run on systems that have multiple cores with multiple threads running on each core. In order to address this problem, the boffins at Cadence started with a clean slate and created a distributed multiprocessing technology that was designed from the ground up to take full advantage of multiple cores—both central processing units (CPUs) and graphical processing units (GPUs).

About 18 months ago, the folks at Cadence released the original Clarity 3D Solver, which is based on an algorithmic approach known as the Finite Element Method (FEM). I don’t know about you, but I’m a bear of little brain and I’m easily confused, so I tend to think of this tool as the “Clarity 3D (FEM) Solver” so as to distinguish it from the “Clarity 3D Transient Solver” in my poor old noggin. The Clarity 3D (FEM) Solver takes full advantage of Cadence’s distributed multiprocessing technology to deliver virtually unlimited capacity and 10X the speed of legacy 3D FEM field solvers while maintaining gold-standard accuracy. This solver is most commonly used as part of a flow in which it is employed to create highly accurate S-parameter models that can be used by other tools and simulators to perform signal integrity (SI), power integrity (PI), and electromagnetic compliance (EMC) analysis.

By comparison, the recently released Clarity 3D Transient Solver—which also takes full advantage of Cadence’s distributed multiprocessing technology to deliver virtually unlimited capacity—is based on a different numerical method called the finite difference time domain (FDTD), which allows us to apply stimulus, observe the results, and visualize transient electromagnetic fields in glorious technicolor. Just how powerful is this? Well, as one simple example, when working with traditional tools, many developers employing DDR memory in their design may be limited to simulating just one or two signal pairs. By comparison, using Clarity, the same developers could simulate the entire DDR bus, which would already put them light-years ahead. Even better, they could model the entire DDR bus in the context of the rest of the system, which would be simply unimaginable with legacy tools.

One thing that really excited me was learning that the Clarity 3D Transient scales in an almost linear fashion. If you have only a single core, a simulation will take a certain amount of time. With two cores, the same simulation will take half the

Figure 1: A variety of simulations are available with the Clarity 3D Transient Solver, which builds on the success of their 3D Field Solver.
time. This math is so simple even I can wrap my brain around it. Suppose you are running a Clarity simulation that takes three days using 32 cores. In this case, if you throw 320 cores at the problem, the simulation will run up to 10X faster.

Where are all these cores coming from? Well, you can use your own on-premises distributed computing solution if you wish. Alternatively, by making their tools cloud-friendly, Cadence has provided the option for essentially unlimited scaling, which means essentially unlimited capacity.

The Clarity 3D Transient Solver produces results for voltage, current, field distribution, and field animation in the time domain. For frequency domain output, results include specific absorption rate (SAR), near/far field distribution, current distribution, and more.

In addition to being able to import mechanical structures from all major MCAD tools (thereby facilitating the modeling of enclosures), the Clarity 3D Transient Solver can easily read design data from all standard chip, IC package, and PCB platforms. Having said this, the Clarity 3D Transient Solver offers integration with Cadence’s own tools, such as Virtuoso Layout, SiP Layout, and Allegro PCB Designer.

Cadence’s Brad Griffin has noted that he and his colleagues have been working with an electronic equipment design, manufacturing, and evaluation company called Ultimate Technologies in Japan. The folks at Ultimate Technologies undertake a lot of engine control unit designs for Japanese automobile manufacturers. According to Brad, they say that the design cycle for a new ECU is typically 10 to 12 months, but by using the Clarity 3D Transient Solver they can literally cut up to three months off each design cycle, which is a more-than-significant achievement.

As Kevin Morris noted in a recent EE Journal column, “They say there are two types of engineers—one who design antennas on purpose, and those who design them by accident.” This is so true, which means that for anyone designing today’s incredibly complex systems with test-measurement accuracy, the Clarity 3D Transient Solver really is “that rainbow they’ve been praying for.”

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