Protocol IP

Accelerating the Deployment of Next-Generation Intelligent Systems

Overview

Cadence is a leader in semiconductor IP, addressing artificial intelligence and machine learning (AI/ML), hyperscale computing, enterprise, data center, and automotive applications. With a comprehensive IP portfolio that includes industry-leading Interface IP, such as high-speed SerDes, advanced memory interfaces, and chiplet IP, Cadence will help you accelerate the deployment of your next-generation intelligent systems. Offering the most advanced foundry processes, Cadence will help you improve your time to market and reduce your costs while ensuring optimal performance, power, and area.

	Protocol	Artificial Intelligence/ Machine Learning	Automotive	Consumer Devices & IoT	HPC, Enterprise, Cloud, and Data Center Solutions	Aerospace/Defense
Ultra Ethernet/Ethernet	224G-LR for UALink (200G/400G/800G/1.6T)				✔	
	224G-LR (200G/400G/ 800G/1.6T)	✔			✔	✔
	112G-VSR (100G/200G/400G/800G)	✔			✔	✔
	112G-LR (100G/200G/ 400G/800G)	✔			✔	✔
	56G-LR (100G/200G/400G)	✔			✔	✔
	SerDes 16G, 16G-MP	✔			✔	✔
	10GBase-KR	✔	✔	✔	✔	✔
	USXGMII/QSGMII/SGMII	✔	✔	✔	✔	✔
PCIe and CXL	PCIe 7.0/CXL	✔			✔	
	PCIe 6.0/CXL	✔			✔	✔
	PCIe 5.0/CXL	✔	✔		✔	✔
	PCIe 4.0		✔	✔	✔	✔
	PCIe 3.1		✔	✔	✔	✔
	PCIe 2.1		✔	✔	✔	✔
	PCIe 1.1		✔	✔	✔	✔
D2D	40G UltraLink D2D			✔	✔	✔
	32G UCIe	✔	✔	✔	✔	✔
	16G UCIe	✔	✔	✔	✔	✔
USB	USB4		✔	✔	✔	✔
	USB 3.0/3.1/3.2		✔	✔	✔	✔
	USB2.0		✔	✔	✔	✔
	eUSB2 v1/v2		✔	✔	✔	✔
MIPI	MIPI D-PHY v1.2		✔	✔		
	MIPI C/D PHY		✔	✔		
	MIPI I3C		✔	✔	✔	✔

	Protocol	Artificial Intelligence/ Machine Learning	Automotive	Consumer Devices & IoT	HPC, Enterprise, Cloud, and Data Center Solutions	Aerospace/Defense
SATA	SATA 3.0 Host				✔	
DDR/LPDDR/GDDR	DDR5				✔	✔
	DDR4			✔	✔	✔
	DDR3			✔		✔
	LPDDR6*	✔	✔	✔	✔	✔
	LPDDR5/5X	✔	✔	✔	✔	✔
	LPDDR4/4X		✔	✔	✔	✔
	GDDR7	✔	✔		✔	
	GDDR6	✔	✔		✔	
High Bandwidth Memory	High Bandwidth Memory (HBM4*) PHY	✔			✔	
	High Bandwidth Memory (HBM3E) PHY	✔			✔	
	High Bandwidth Memory (HBM2E) PHY	✔			✔	
Storage	xSPI		✔	✔	✔	
	SD/eMMC		✔	✔		
	ONFi/Toggle		✔	✔		

*JEDEC standards are subject to change during and after the development process, including disapproval by the JEDEC Board of Directors.

Table 1: Applications supported by protocol

Advanced SerDes

We offer various complete, configurable, and production-proven interface protocols, such as Ethernet, PCIe, UCIe, CXL, D2D, USB, SATA, DP, and MIPI. All these solutions are designed with your SoC in mind, eliminating the need for you to design around our IP. Moreover, our IP can be delivered with a complement of Cadence Verification IP (VIP) and models. Pre-verified solutions

			TSMC							Samsung					Intel	Rapidus	Global Foundries			Controller
	Protocol	Data Rate	22ULP/28HPC+	16/12FFC	N7/N6	N5/N4P	N5A	N3E/N3P	N3A	14LPP	8LPP/10LPP	7LPP	SF5A	SF4X	18A	2nm	14/12LP	12LP+	22FDX	
Ethernet	224G-LR for UALink (200G/400G/800G/1.6T)							✔							✔					
	224G-LR (200G/400G/ 800G/1.6T)	212.5 Gbps						✔								✔				✔
	112G-VSR (100G/200G/400G/800G)	112 Gbps						✔												✔
	112G-LR (100G/200G/ 400G/800G)	106.25G/112 Gbps			✔	✔		✔					✔							✔
	56G-LR (100G/200G/400G)	53.125 Gbps			✔															✔
	SerDes 32G-LR/MP	32Gbps																	✔	
	SerDes 30G-MR/VSR	30Gbps															✔			
	SerDes 28G-LR	28Gbps								✔							✔			
	SerDes 28G/25G-MR	28Gbps								✔							✔			
	25G-KR (25G/100G)	25.78125 Gbps			✔	✔	✔	✔	✔	✔							✔		✔	✔
	SerDes 16G, 16G-MP	16Gbps		✔	✔	✔				✔	✔						✔			✔
	10GBase-KR	10.3125Gbps	✔	✔	✔	✔	✔	✔	✔	✔	✔						✔		✔	✔
	USXGMII	10.3125Gbps		✔	✔	✔	✔	✔												✔
	QSGMII	5Gbps	✔	✔	✔	✔	✔	✔												✔
	SGMII	1.25Gbps	✔	✔	✔	✔	✔	✔	✔											✔
	Multi-Speed Ethernet Controller (soft IP)	10M/100M /1G																		✔
PCIe and CXL	PCIe 7.0/CXL	128Gbps				✔		✔								✔				✔
	PCIe 6.0/CXL	64Gbps				✔		✔	✔				✔		✔					✔
	PCIe 5.0/CXL	32Gbps			✔	✔	✔	✔	✔				✔	✔						✔
	PCIe 4.0	16Gbps		✔	✔				✔	✔	✔						✔	✔	✔	✔
	PCIe 3.1	8Gbps	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔				✔		✔	✔
	PCIe 2.1	5Gbps	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔				✔	✔	✔	✔
	PCIe 1.1	2.5Gbps	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔				✔	✔	✔	✔

✔ *Ready for design*
✔ *In progress*

			TSMC							Samsung					Intel	Global Foundries		Controller	
CPR/eCPRI	Protocol	Data Rate	22ULP/28HPC+	16/12FFC	N7/N6	N5/N4P	N5A	N3E/N3P	N3A/N3AE	28 FD-SOI	8LPP/10LPP	7LPP	SF5A	SF4X	18A	12LP+	22FDX		
	CPRI	24.33 Gbps			✔	✔		✔									✔		
D2D	40G UltraLink D2D	40Gbps			✔	✔		✔				✔				✔		✔	
	UCIe	32Gbps						✔										✔	
	UCIe	16Gbps			✔	✔	✔	✔	✔				✔		✔			✔	
USB	USB4	2x20Gbps		✔		✔	✔												
	USB 3.2	2x10Gbps	✔	✔	✔	✔	✔	✔	✔		✔	✔	✔		✔			✔	Host/Device
	USB 3.1	10Gbps	✔	✔	✔	✔	✔	✔	✔		✔	✔	✔		✔			✔	
	USB 3.0	5Gbps	✔	✔	✔	✔	✔	✔		✔	✔	✔	✔					*	
	USB2.0	480Mbps	✔	✔	✔					✔		✔	✔					✔	OTG
	eUSB2v1	480Mbps			✔	✔	✔											✔	OTG
	eUSB2v2	4.8Gbps	✔					✔							✔			✔	Host/Device
MIPI	C/D PHY 2.x/2.1	3.5Gsps - 6Gsps/ 4.5Gbps			✔	✔												✔	CSI-2/DSI/DSI-2
	C/D PHY 1.x/1.2	2.5Gsps -3.5Gsps/ 2.5Gbps	✔	✔	✔													✔	
	D-PHY v1.2	2.5Gbps	✔	✔	✔													✔	
	I3C	Soft IP																✔	
SATA	SATA 3.0 Host	6.0Gbps		✔	✔	✔	✔	✔	✔				✔						
DP 1.4 TX	DP 1.4 TX	8.1Gbps		✔	✔	✔	✔	✔	✔				✔						

Table 2: IP for Ethernet, PCIe and CXL, and D2D connectivity

✔ *Ready for design*
✔ *In progress*
* *DRD/HCI host only*

save time and effort and allow you to focus on your innovative designs.

Advanced Memory

We offer the broadest and most configurable portfolio of the industry's widely used memory and storage protocols. The Cadence Denali® Memory IP gives you the added value of multi-standard DDR support by providing controller IP that supports DDR5, DDR4, DDR3, DDR3L, LPDDR5X/5, LPDDR4X/4, and LPDDR3 as a single IP solution, as well as GDDR6. We also offer

		TSMC								Samsung							Intel	Rapidus	Global Foundries				Controller
Protocol	Perf. (Mbps)	22ULP	28HPC+	16FFC	12FFC	N7/N6	N5/N4P	N3E/N3P	N3A	11nm	14LPP	8LPP	7LPP	4LPP	5LPE	SF4X	18A	2nm	14/12LP	12LP+	22FDX	28SLP	
GDDR7	36Gbps						✔	✔								✔							
GDDR6 PHY	22+G						✔																✔
	16G					✔	✔				✔	✔	✔		✔	✔			✔	✔			✔
DDR5/4	12.8Gbps						✔	✔															✔
	8,800+						✔	✔							✔	✔							✔
	6,400+						✔	✔							✔								✔
	5600						✔								✔								✔
	4800			✔	✔	✔	✔						✔							✔			✔
LPDDR5X/5	9600					✔	✔	✔	✔								✔						✔
LPDDR5/4X	6400					✔	✔																✔
DDR5/4, LPDDR5/4X combo	5600					✔	✔							✔						✔			✔
LPDDR4/3/DDR4/e[L]	4266	✔	✔	✔	✔	✔																	✔
LPDDR4/4X/3/DDR4	4266			✔		✔																	✔
DDR4/3[L]	3200	✔	✔	✔	✔	✔																	✔
DDR 4 Multi-modal PHY	3.2Gbps																		✔	✔			✔
DDR 4 PHY	3.2Gbps										✔								✔	✔			✔
DDR 4/3	3.2Gbps/2.133Gbps																		✔				✔
DDR3 PHY	2.133Gbps																		✔	✔		✔	✔
High Bandwidth Memory (HBM4)								✔										✔					
High Bandwidth Memory (HBM3E) PHY	9.6Gbps/10.4Gbps					✔	✔	✔															✔
High Bandwidth Memory (HBM2E) PHY	3.6G					✔				✔									✔	✔			✔

Table 3 : Advanced Memory

✔ *Ready for design*
✔ *In progress*

high-bandwidth memory (HBM) as well as advanced memory IP solutions created by the best experts in the field to provide you with the controller, PHY, and VIP you need for your design.

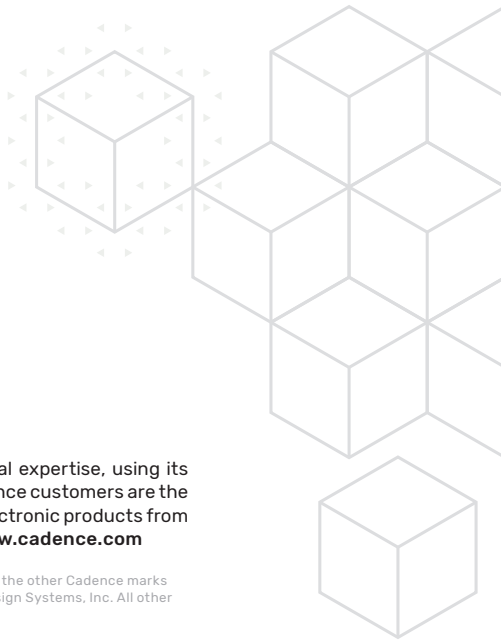
Storage IP

Cadence storage IP solutions consist of three popular technologies: NAND Flash, SD/eMMC, and xSPI. These memory technologies address the needs of a broad range of market requirements. The Cadence NAND Flash Controller IP supports all major NAND Flash manufacturers handling asynchronous devices and meets many standards. The Cadence NAND Flash PHY IP is available as soft IP with a delay-locked loop (DLL), a firm PHY, or a hard PHY for your specific process and library. The Cadence SD/eMMC IP is compliant with the latest versions of Secure Digital and Embedded Multimedia Memory Card standards, which makes our IP the perfect choice for both high-performance and low-power solutions. The Cadence xSPI IP is compliant with a range of serial standards.

	Protocol	Soft PHY	TSMC 16/12 FFC	TSMC N7	Ctrl
xSPI	xSPI - Supports multiple serial standards including OSPI and QSPI	✔			✔
SD/eMMC	SD 6.0/eMMC5.1	✔			✔
	SD 4.0/eMMC5.1	✔			✔
NAND	ONFI4.x/Toggle 2	✔			✔
	ONFi 5.x Firm PHY and I/O / Hard PHY		✔	✔	
Combo	Multistandard PHY supporting NAND, SD/eMMC, and xSPI	✔			✔

Table 4: IP for storage

✔ *Ready for design*
✔ *In progress*



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