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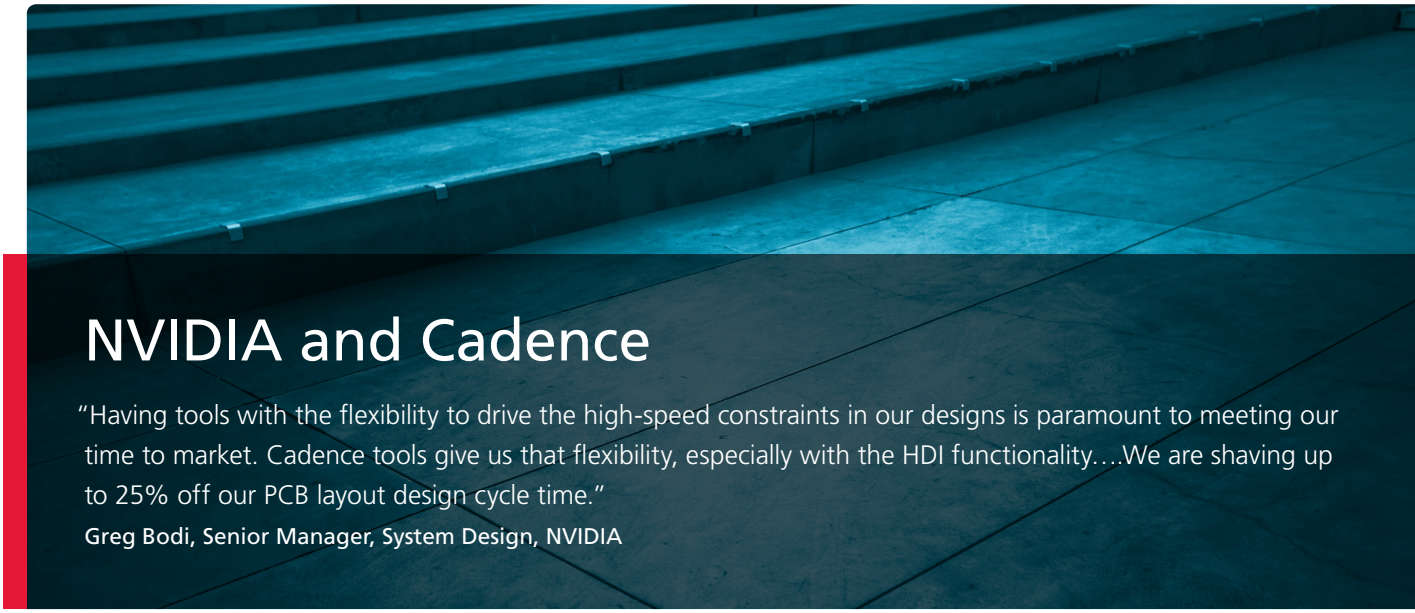

NVIDIA and Cadence

"Having tools with the flexibility to drive the high-speed constraints in our designs is paramount to meeting our time to market. Cadence tools give us that flexibility, especially with the HDI functionality….We are shaving up to 25% off our PCB layout design cycle time."

Greg Bodi, Senior Manager, System Design, NVIDIA

The Customer

NVIDIA leads the industry in developing visual computing technologies and is the inventor of the GPU, a high-performance processor that generates breathtaking, interactive graphics on personal computers, game consoles, and mobile devices such as smartphones.

The Challenge

To keep up with consumer demand for such high-performance gadgets, NVIDIA must meet stringent time-to-market windows. The company's average design cycle is less than six months, from silicon tapeout to printed circuit boards (PCBs) ready for the marketplace.

NVIDIA design teams were using Cadence tools to create their IC package and board designs. They had also developed several in-house tools for ball grid array (BGA) fanout and routing to augment their existing Cadence® Allegro® constraint-driven PCB design flow. But the pressures of product miniaturization and high-density interconnect (HDI), combined with an increasing number of constraints, was creating new challenges.

"NVIDIA designs require a robust, constraint-driven PCB design flow," explains Greg Bodi, NVIDIA Senior Manager, System Design. "Having HDI capabilities driven by that flow is critical for us to meet our time-to-market objectives."

The question was whether to invest time and resources developing tools to enable HDI, or to adopt a new solution. And since NVIDIA was designing with high-speed constraints but also using "build-up" technology to handle BGA fanout, they would need a highly flexible solution that could address both sets of requirements.

Business Challenges

- Tight six-month time-to-market windows
- Product miniaturization requires more in-house design tools and skills to optimize high-density interconnect (HDI)

Design Challenges

- Handle HDI combined with an increasing number of constraints
- Drive micro vias quickly and accurately
- Reduce the number of layers on customers' boards
- Shorten the overall PCB layout design cycle

Cadence Solution

- HDI-enabled, constraint-driven PCB design flow
- Allegro PCB Design technologies

Results

- High-speed, constraint-driven HDI flow shortened the PCB design cycle by 25%
- Unified PCB design, layout, editing, and routing technologies mitigated risk, boosted performance, and increased efficiency
- Collaboration with NVIDIA engineers streamlined time to productivity with the enhanced flow

The Solution

NVIDIA decided to migrate to the latest Allegro PCB Design technologies, which starting with the 16.2 release enable a constraint-driven HDI design flow.

Having worked with Cadence before, NVIDIA felt assured that adopting the new flow would be easy and that collaboration with Cadence would optimize their time to productivity.

The new Cadence flow combines the proven Allegro constraint-driven PCB design flow with a comprehensive set of automation-assisted manufacturing rules for all different styles of HDI designs, from a hybrid build-up/core combination to a complete build-up process.

"Having tools with the flexibility to drive the high-speed constraints in our designs is paramount to meeting our time to market," Bodi says. "Cadence tools give us that flexibility, especially with the HDI functionality."

"We have an extremely strong relationship with Cadence, which has one of the best engineering support systems I've seen. Cadence is diligent about making sure NVIDIA is a successful company."

In particular, Allegro PCB Editor now includes automation for adding and managing micro vias to shorten the time to create designs that are correct-by-construction. From front-end design creation to signal integrity to back-end layout, the Allegro 16.2 release boosts productivity and predictability while streamlining the product development cycle.

Shorten the PCB design cycle by 25%

HDI designs are extremely complicated to develop, fabricate, and assemble because of the small pitches on the components. Allegro PCB Design technology for HDI designs includes an extensive set of new HDI rules for micro vias and same-net elements, an enhanced via-transition use model, via stacking rules, and powerful automation-assisted interconnect and via pattern insertion.

Manufacturing IP-driven wirebonding and co-planar waveguide modeling further boost productivity and reduce engineering change orders (ECOs). Enhanced capabilities to partition the design horizontally and add soft boundaries allows users to work in parallel more efficiently and speeds the design cycle.

For NVIDIA, the key advantage of the Cadence HDI functionality is the ability to handle micro vias—blind and buried vias, how the vias are built, and how they affect the lamination cycle.

"Cadence has done a lot of good engineering work to come up with a methodology for driving down the micro vias through the layers to get the correct via structure, spacing for the vias themselves, through-hole vias, and to other metal shapes and traces in a design," Bodi explains. "We are shaving up to 25% off our PCB layout design cycle time for complex high-speed designs that use HDI technology."

NVIDIA's designs require certain spacing from one micro via to an adjacent micro via or blind/buried via. In the past there was nothing to control that, but with the new Cadence HDI functionality, it can be done on-the-fly.

The Cadence solution automatically drops the vias in the correct location, which greatly increases efficiency and eliminates previous user-developed and user-maintained workarounds. Now that the NVIDIA team has an integrated HDI design and validation mechanism, they don't have to spend time building internal automation tools or performing post-processing. Nor do they need to build their own workaround to develop ways to keep the correct spacing, which applies to both IC package substrate design and PCB HDI design.

Another key enhancement in the 16.2 release is more flexibility to handle HDI design specifically when it comes to constraints for HDI. With the proven Cadence constraint-driven flow, electrical engineers can specify physical and spacing constraints for critical high-speed nets and embed those in the design to improve the chances of first-time success. These constraints are required for signals such as those found in memory interfaces (DDR2/DDR3), where the engineer needs to specify line widths and spacing to manage impedance and shield critical signals from crosstalk.

"We need to know what our signal integrity and power delivery is going to be like," Bodi says. "Some of our products have designs with currents up to 200 amps. The Cadence solution fits the high-speed design flow with good signal integrity."

NVIDIA also uses the built-in Allegro Field Solver to push the correct impedances into their designs and to eliminate unnecessary iterations between hardware designers and PCB layout designers. After pushing the correct impedances, they enter numbers quickly into the Allegro Constraint Manager flow and start the design.

Optimize time to productivity

Throughout the development process, Cadence technology experts worked with the NVIDIA team to address their concerns about any new design processes or tools. This collaboration allowed NVIDIA to quickly incorporate the enhanced flow and solution capabilities, helping them to further streamline the design cycle and meet their market window.

"We have an extremely strong relationship with Cadence, which has one of the best engineering support systems I've seen," Bodi explains. "They do a good job of listening to our concerns and our enhancements requests. Cadence is diligent about making sure NVIDIA is a successful company."

Summary

NVIDIA used Allegro technology to enable shorter, more predictable design cycles for its PCB designs. And now with a constraint-driven HDI design flow, NVIDIA can develop even smaller boards with fewer layers and higher performance to stay on top of the competitive and price-sensitive consumer electronics market.