

ConnX Family of Radar, Lidar, and Communications DSPs

Configurable, extensible, scalable

The Cadence® Tensilica® ConnX family of enhanced digital signal processors (DSPs) establishes a new standard in high-performance, low-power digital signal processing specifically designed for radar, lidar, and communications processing. Optimized for complex number processing, the ConnX DSPs offer a wide range of software-compatible power, performance, and area (PPA) points to suit the needs of any application. These DSPs provide the scalability needed to deliver energy-efficient programmable solutions for radar, lidar, and communications applications (such as infrastructure, user equipment, IoT, and V2X). Easily optimized through check-box options, the ConnX DSPs provide unprecedented flexibility in implementing systems at power consumption levels that significantly reduce the need for hardware accelerators. The five members of the family include ConnX BBE16EP DSP, ConnX BBE32EP DSP, ConnX BBE64EP DSP, ConnX B10 DSP, and ConnX B20 DSP.

Features

Throughput	Tensilica ConnX DSPs				
	BBE16EP	BBE32EP	BBE64EP	B10	B20
Vector/Memory width (b)	128	256	512	256	512
MACs 16bx16b	16	32	64	64	128
MACs 32bx32b	-	-	-	16	32
SP FP FMA	4	8	16	16	32
HP FP FMA	-	-	-	32	64
DP FP FMA	-	-	-	8	16
ALU 8b	-	-	-	96	192
ALU 16b	24	48	96	48	96
ALU 32b	4	8	16	32	64
Divider 16b	1	2	4	2	4
Divider 32b	-	-	-	1	2

Notes:

MAC: Multiply-accumulate operation
 FMA: Fused multiply-add operation
 ALU: Arithmetic logic unit
 SP FP: Single-precision floating point
 HP FP: Half-precision floating point
 DP FP: Double-precision floating point

- ▶ Single-instruction, multiple-data (SIMD) vector processing
- ▶ Very long instruction word (VLIW) for parallel load/store, MAC, and ALU ops
- ▶ 32-bit scalar ALU
- ▶ Higher precision for matrix inversion and divide operations
- ▶ Optimized instructions for:
 - 16b: Complex arithmetic
 - 16b: Polynomial evaluation
 - 16b: Matrix multiplication
 - 16b and SP: FFT and RECIP/RSQRT acceleration
 - 16b: FIR, convolution, correlation acceleration
 - 16b and 32b: Peak search acceleration

- SP: Block floating point
- Bit-oriented operations
- Vector compression and expansion
- ▶ Predicated vector instructions
- ▶ Vector single-precision floating-point option
- ▶ For the ConnX B10/B20 DSPs
 - Faster clock speed compared to the ConnX BBE DSPs
 - 16b: sin / cos / complex exponent acceleration
 - Optional 32b vector fixed-point MAC for FFT, FIR, convolution, correlation, and more
 - Optional extended-vector single-precision floating point for 2X SP performance
 - Optional extended-vector half-precision floating point
 - Optional extended-vector double-precision floating point
 - Optional communications acceleration for forward error correction (FEC)
 - Multicore solution
- ▶ High-performance C/C++ compiler with automatic vectorization of scalar C and full support for vector data
- ▶ TI intrinsic support, rich math libraries

Benefits

- ▶ Certified as ISO 26262:2018 ASIL-compliant and suitable for use in safety-critical automotive applications.
- ▶ High performance, low power over a broad range of algorithms including support for radar, lidar, and communications (5G, 4G, LTE Advanced, LTE, HSPA+, and Wi-Fi)
- ▶ Fast development through familiar C programming in an Eclipse-based IDE along with optimized math libraries and application examples with source
- ▶ Full support for hardware/software co-design
- ▶ Easy integration into SystemC® simulations with functional, cycle-accurate, and hardware pin-level models
- ▶ Configurable— Multiple pre-verified vector packages to select from
- ▶ Extensible—Customizable instruction set through the Verilog-like Tensilica Instruction Extension (TIE) language, with virtually unlimited bandwidth from FIFO, GPIO, and lookup interfaces
- ▶ Scalable—Software-compatible DSP family, making evaluation/migration easy

High Performance, Energy Efficient, Maximum Flexibility

Fast time to market, evolving standards, and long platform lives are all incompatible with the rigidity of ASIC-based designs for next-generation products. Whether it's a product targeting a 5G communications microcell, access point, mobile hotspot, tablet, smartphone, car-2-car, car-2-infrastructure, or a higher resolution imaging radar sensor or a lower-cost solid-state lidar, they all benefit from the flexibility of a software-based solution as these markets develop and mature. This flexibility can only be achieved by implementing parts of the signal processing chain on programmable processors.

The ConnX DSPs are built on Cadence's proven Tensilica Xtensa® customizable processor architecture and are specifically designed to support the needs of radar, lidar, and communications signal processing. They deliver the processing capacity needed in single- and multi-core systems with an instruction set specifically targeted at the processing requirements in these markets. As needed, hardware blocks may be interfaced to the Tensilica ConnX processors via dedicated custom interfaces under the ConnX processor control or as initiator/responders via the system bus interfaces or via shared memory.

Beyond simple software programmability, support for push-button assembly of optimized processors is at the heart of all Xtensa-based ConnX products. This includes the ability to:

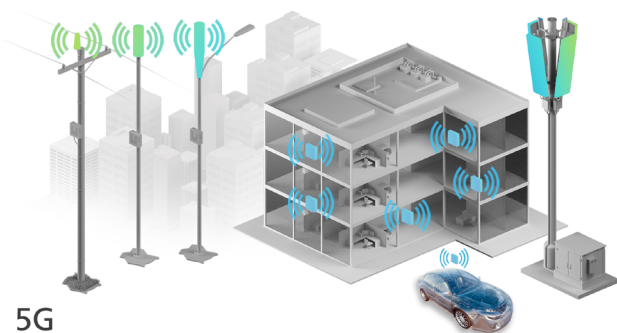
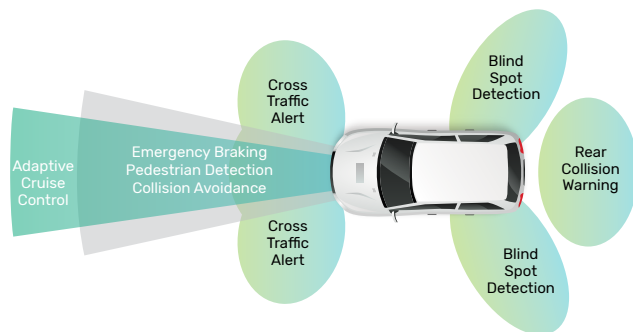
- ▶ Integrate pre-verified function blocks to add to the basic instruction set, if needed
- ▶ Add new custom instruction hardware (with full C tool support added automatically), if needed
- ▶ Integrate into complex systems through a variety of general-purpose and performance-optimized interfaces.

Whether implemented as a single core, as an array of ConnX DSPs or a hybrid system on chip (SoC) made up of a diverse mix of ConnX processors and hardware accelerator blocks, the ConnX DSPs are there to do the heavy lifting at the intersection of maximum performance, low energy, and design flexibility.

Configurable, Extensible, Scalable

The Tensilica ConnX DSPs provide pre-verified accelerator instruction options. These options are included/excluded as checkboxes when defining a core and result in the seamless integration of that feature into the hardware, the compiler, the modeling tools, and the verification scripts. With these capabilities, you can build a custom DSP without the large development schedule impact that a change in hardware design would normally involve.

The ConnX DSPs can be extended to support custom ports and queues for efficient, direct, connection to offload accelerators and are fully supported in the programming and modeling tools. These custom interfaces can be defined to match the interfaces of existing third-party IP. Thus, the ConnX DSPs can access hardware offload accelerators in a deterministic single- or multi-cycle operation, greatly reducing power consumption and without impacting the shared system bus.



Application Space: Radar, Lidar, 5G Communications

The Tensilica ConnX family products are high-performance DSPs designed for next-generation radar, lidar, and communication systems (including legacy support for 4G, LTE Advanced, LTE, WCDMA, HSPA+, Wi-Fi, and DVB). Higher precision options are specifically designed to meet the accuracy and performance requirements associated with the advanced MIMO systems needed. In addition to vector-based filtering, FFT, and linear algebra-processing capabilities, a fully featured instruction set includes a full range of bit-oriented operations. The ConnX processors excel at running control code and are used to perform the PHY application layer control in addition to digital signal processing, providing opportunities for hardware savings and a broader scope of applications than a dedicated fixed hardware solution could provide.

As physical layer (PHY) system developers move to advanced standards such as 5G, and radar system developers add more antennas for higher resolution, they face the need for dramatic increases in performance from their processing platforms. The ConnX DSPs meet this challenge with their highly parallel vector engines and, with compatible architectures, provide an easy upgrade path to other ConnX family members when needed. If processing needs scale beyond that of a single DSP, the ConnX family provides smooth support for multi-core solutions.

As systems become more diverse with wide-scale deployment of heterogeneous networks, the solution that may work best for a microcell operating on a bullet train in Japan may be very different from a similar microcell operating in a subterranean pedestrian mall in downtown Montreal. A programmable software-based solution using a ConnX DSP allows you to implement both solutions on a single platform and allows it to evolve without going back for an expensive and time-consuming respin of the silicon.

With a solution based on a ConnX DSP, you can deliver a working solution in less time than a traditional hardware or a hybrid hardware/DSP design. You can also deploy this programmable hardware platform for a broader range of applications and over a longer period of time. Ultimately, this reduces costs and results in a faster time to market, helping you deliver more competitive solutions in the marketplace.

Toolchain

The Tensilica ConnX DSPs are delivered with a complete set of software tools. The toolset includes a high-performance C/C++ compiler with automatic vectorization and instruction bundling to support the VLIW pipeline in the DSP. This comprehensive toolset also includes the linker, assembler, debugger, profiler, and graphical visualization.

A comprehensive instruction set simulator (ISS) allows you to quickly simulate and evaluate performance. When working with large systems or lengthy test vectors, the fast, functional TurboXim™ simulator option achieves speeds that are 40X to 80X faster than the ISS for efficient software development and functional verification.

Xtensa SystemC (XTSC) and C-based Xtensa Modeling Protocol (XTMP) system modeling are available for full-chip simulations. Pin-level XTSC offers co-simulation of SystemC and RTL-level offload accelerator blocks for fast, cycle-accurate simulations.

The ConnX DSPs support all major back-end EDA flows, and represent the ultimate in customizable DSPs from Cadence, the leader in configurable, extensible, and scalable solutions for advanced radar, lidar, and communications systems. This proven development environment for both hardware and software reduces time to market and risk, as well as providing maximum flexibility in processing solutions for radar, lidar, communications, and beyond.

The Cadence logo consists of the word "cadence" in a lowercase, sans-serif font. The letter "a" is stylized with a horizontal bar above it. A registered trademark symbol (®) is located to the upper right of the "e".

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