

How IP Drives More Integrated Features in Mobile Systems

Cadence

It's human nature that we are never satisfied, and so it goes with our expectations for mobile devices. We want more functionality, more integrated features, more hands-free operation, longer battery life. The list goes on. For designers, it's a tall order to meet, but one that can be managed by designing with the right third-party or commercial intellectual property (IP). This paper discusses how design, verification, and optimizable processor IP can help you meet the power, performance, area, and time-to-market targets for advanced-node mobile designs.

Contents

Introduction	1
IP Supports Focus on Product Differentiation	2
Key Protocols for Mobile Designs	3
Analog IP	4
Verification IP	4
Optimizable Processor IP	4
Cadence IP Streamlines Mobile Design Cycle	5
Optimizing Electronic System Design	5
Summary	6
For More Information	6

Introduction

As shown in Figure 1, BI Intelligence estimates a fairly robust global market outlook for Internet-connected mobile devices: 2.4 billion smartphones and 676 million tablets by 2018, up from 1.3 billion smartphones and 314 million tablets in 2014. Databeans anticipates that the mobile market will rise from \$77 billion in 2012 to \$141 billion in 2018. As expectations have changed, the requirements for these mobile systems have grown much more complex.

Not only do many consumers now carry multiple mobile devices, they also want these devices to do more processing-intensive tasks, from making payments to streaming HD videos and playing games. For some, the mobile phone is their primary computer, providing fingertip access to a wealth of information and capabilities that promote productivity, enhance relationships, and much more. Users want their mobile experience to be smooth and seamless across their different devices, from smartphones to tablets to smartwatches. And, of course, they want each charge to last a long time, along with sophisticated hands-free operation and minimal reliance on cables with different connectors.

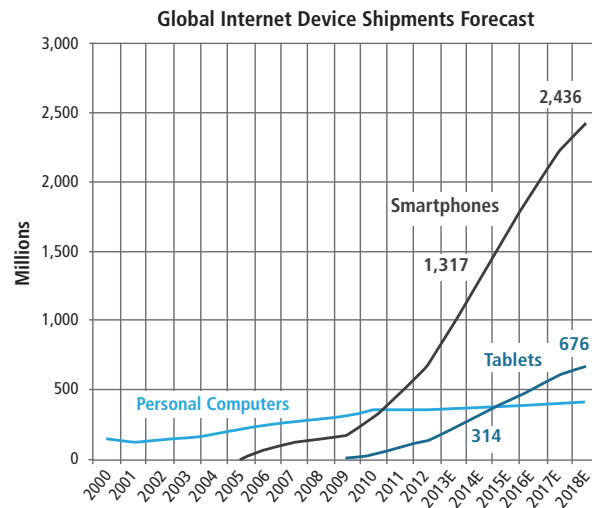


Figure 1: Smartphone and tablet market projects, from 2000 to 2018. Source: BI Intelligence

Mobile is at the forefront of innovating use models, since we interact with these devices in a variety of ways (voice, gestures, vision, etc.). What's needed to make all of this possible? These capabilities are now essential for mobile systems:

- Increased memory size/bandwidth and lower latency
- Lower power consumption
- Unified cable/connector solution
- Lower power gesture and voice recognition via always-on capabilities

Enabling these functionalities is where IP really shines. With pre-verified IP, you can streamline your development and verification cycle and meet your power budget while delivering the features that consumers now expect in a timely manner. Designing with the right IP, you can meet aggressive market windows without having to worry about keeping up with constantly changing design protocols. Design IP and verification IP have protocol knowledge built-in. The value in having verification IP in the mix is not so much to verify the design IP, as it should already be verified. Verification IP helps to verify that your system—the mobile device—works with each protocol as intended.

IP Supports Focus on Product Differentiation

Smartphone and smartwatch application processors are continuing to be developed using multi-core embedded processors at advanced-node processes, including FinFET processes. Tablet application processors are following a similar pattern. Long-Term Evolution is no longer a differentiator; differentiation now lies in features as well as modem carrier certification.

Most smartphones boast a single chip integrating the application processor and the cellular baseband. We anticipate that by 2017, there will be no standalone application processors in smartphones. And by 2018, we anticipate that 30% of tablets will use the integrated application processor plus baseband chips. There are many other components to consider besides application processors and baseband chips: multiple PMICs, WiFi connectivity modules, touch controllers, RF amplifiers, transceivers, and MEMs (including compass and accelerometers). IP cores can support the development of each of these components.

In fact, IP continues to take on a greater role in chip design, as pre-verified IP can contribute to faster time to market, product differentiation, and lower overall costs. According to MarketsandMarkets, the semiconductor IP market is projected to reach \$5.63 billion in 2020, growing at a CAGR of 12.6% from 2014 to 2020.

Standards-based design IP lets you manage IP-to-SoC development in a system context, so you can focus internally on differentiation and take advantage of multi-function IP to do more and get it done faster. In other words, IP lets you get some time and bandwidth back on your plate. Verification IP streamlines the effort of ensuring that your

designs comply with various specifications and that the IP is operating properly in the context of the system. Small, low-power, configurable DSPs can enable always-on functionality such as voice triggering and face detection in smartphones and tablets.

Key Protocols for Mobile Designs

Let's highlight some of the key protocols that are important for mobile system designs. Design interface IP that is silicon-proven for standard interfaces can free your resources to focus on product differentiation versus spending time and effort gaining an in-depth understanding of a variety of evolving protocols whose specifications can span hundreds of pages.

SerDes

SerDes IP can address performance, power, and area requirements for mobile systems. Chip-to-chip SerDes supports high-performance data movement between the application processor chip and the modem chip. Support for high data rates is essential for applications like video streaming, while low exit latency is important for time-critical applications. Look for SerDes IP that supports the latest PCI Express®, Ethernet, USB, MIPI®, SATA, and OLT specifications.

LPDDR4

Ideal for power-sensitive consumer and mobile devices, the LPDDR4 memory protocol delivers data rates of up to 25.6Gbps with about 50mW of power per Gbps. Given its performance and power ratio, along with its low-latency data access, LPDDR4 offers what's needed to load and play videos and support cloud/app analysis and storage requirements. With the higher speeds, power and noise can have a larger impact on performance. As you're evaluating LPDDR4 IP, look for IP that can optimize power consumption and efficiently filter out signal noise.

USB Type-C™

Previously, we mentioned how consumers have less tolerance for managing multiple cables with different connectors. USB Type-C Cable and Connector Specification promises to simplify the use and maintenance of a host of electronic devices. The adoption of USB Type-C with USB Type-C Alternate Modes (Alt Modes) and USB Power Delivery specifications allows electronic devices to operate on a single cable for charging, data transfer, and video output. Thanks to these specifications, USB Type-C connectors can support data rates up to 10Gbps and up to 100W of power. In addition, USB Type-C also supports small form factors and, by standardizing cables and connectors, lower cost of ownership. IP for USB Type-C can help you meet the requirements of the standard and also future-proof your design. Figure 2 shows an example of a USB Type-C IP sub-system, which can help streamline the development process for USB Type-C designs with DisplayPort support.

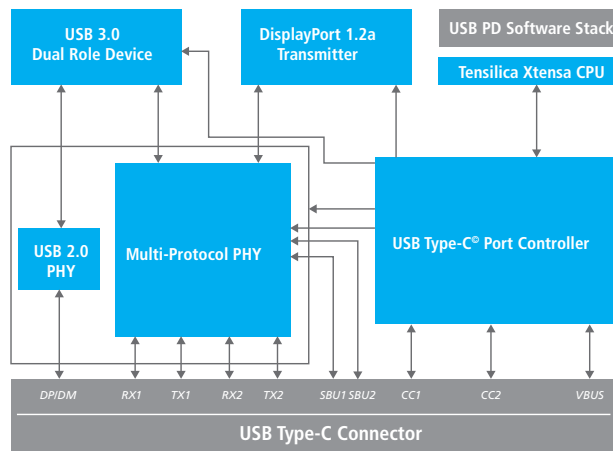


Figure 2: Sample USB Type-C sub-system

MIPI

The latest MIPI Alliance specifications support fast video and audio transmission for next-generation mobile devices. In addition, MIPI specifications are suited for mobile devices as they address the need for low power, low electromagnetic interference, and high-performance operations. The MIPI® M-PHY specification supports high-speed chip-to-chip communications from the application processor of a smartphone or tablet to modems, storage devices, and components like cameras. The right MIPI IP can enable you to include the best available graphics and cameras in lower cost smartphones.

HDMI

High-Definition Multimedia Interface (HDMI) is an audio/video interface for transferring uncompressed video data and compressed or uncompressed digital audio data from an HDMI-compliant source device. Newer versions of the standard offer improved audio/video capacity, performance, and resolution.

Analog IP

Also important for mobile designs are analog IP including analog front ends (AFEs), analog-to-digital converters, power monitors, and thermal sensors. Wireless transceivers that are critical components in an array of mobile devices need to be small and very low power. As such, a successive approximation register (SAR) architecture is ideal for the analog-to-digital converter (ADC) that is a key component of a wireless AFE. The ADC typically consumes the most power in the AFE; as such, choosing an ADC with the lowest power consumption for the targeted specifications would be ideal to extend battery life in a portable device. Data converter IP cores based on the SAR architecture and that support next-generation applications such as WiGig can meet the needs for today's (and tomorrow's) mobile designs.

Verification IP

Considering that specifications for standard interface protocols can be hundreds of pages long, and the protocols continually evolve, keeping up to date might require more effort, time, and resources than you can afford. Verification IP can help you verify your mobile SoC designs faster, more thoroughly, and with less effort (Figure 3). With verification IP, you can model all of the interfaces in your design as components. You can then plug these components into an SoC testbench for simulation along with your chip. You can also tap into memory models to verify interface functionality and timing.

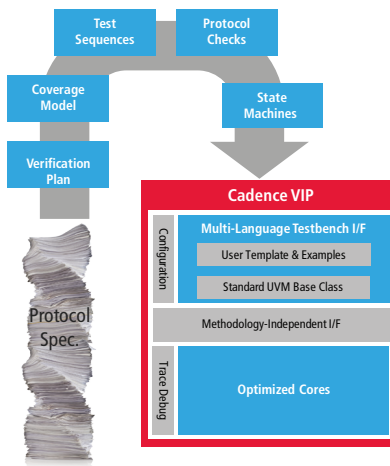


Figure 3: Cadence Verification IP can help simplify the digital simulation of standard interfaces for mobile applications.

Optimizable Processor IP

Optimizing a processor to suit the specific needs of an application increases performance and reduces energy consumption. Always-on functionality such as voice triggering, voice recognition, face trigger, and sensor fusion—capabilities that are especially important in small form factor mobile devices like smartwatches—need this energy efficiency to be feasible. These optimized processors typically offload the main application processor in your design, reducing energy consumption and providing smoother playback for high-performance features such as audio and

video. These processors can also provide imaging and computer vision functionality, convolutional neural network capabilities that enable pattern recognition, and security and decryption (implementing algorithms in a customized processor can make it harder to pirate).

Cadence IP Streamlines Mobile Design Cycle

In its extensive design, verification, and configurable processor IP portfolio, Cadence offers solutions that help streamline the development cycle for mobile applications, supporting the latest protocol specifications as well as advanced-node processes. For example:

- 8G chip-to-chip SerDes IP enables high performance on board data movement
- LPDDR4 IP provides the lowest latency and lowest power data access
- USB Type-C/DisplayPort IP supports unified connectors/cables and high-definition video
- IP for the MIPI protocol supports integration of commodity high-resolution displays and cameras
- HDMI 2.0 simulation verification IP is the industry's first, supporting 3D video formats for 25Hz frames, 4Kx2K resolution, deep color modes, and much more
- Analog IP—including AFEs, ADCs, and digital-analog converters (DACs)—are based on the SAR architecture and provide faster conversion rates with less power consumption and smaller area requirements than competitive solutions
- Tensilica® optimizable processors support a wide variety of predefined functionality targeted at always-on gesture recognition, imaging/computer vision, neural networks for pattern recognition, and audio/speech

These are just a few examples in a portfolio that includes dozens of different IP supported by a strong ecosystem, geared to help you turn your ideas into differentiated mobile products under aggressive development timelines.

Optimizing Electronic System Design

Each of the electronic components within an end product can no longer be designed in isolation if you want the assurance of an optimized design, where all of the pieces work well together and you're able to streamline your design cycle. Cadence's design IP, verification IP, and Tensilica IP are part of a broad portfolio of hardware, software content, and services that help streamline the design and verification of your entire communications/mobile system, from chip to package to board and the final product.

Our IP portfolio is complemented by:

- System design and verification tools that help you concurrently develop the hardware and software components, accelerate IP development, and integrate the SoCs for your mobile design
- Full-flow digital design and signoff platform that helps you meet your power, performance, and area (PPA) requirements with a fast path to design closure and better predictability
- Custom IC/analog/RF design tools that save you time by automating simulation, routing, and library characterization
- IC package design and analysis tools that address signal and power integrity, multi-fabric co-design, and other challenges for system-in-package (SiP), multi-tier wirebond, stacked-die, and other package designs
- PCB design and analysis tools that enable fast, efficient product creation with constraint-driven functions, auto-interactive technologies, support for rigid-flex designs, and capabilities that streamline ECAD/MCAD collaboration

With these integrated design solutions, you can efficiently ensure that each component in your system will function as intended on its own and in conjunction with all of the other components. You can also account for environmental and other operating conditions. In short, with Cadence's system design technologies, you can turn your ideas into compelling, differentiated end products, working productively, reducing risks, focusing on high quality, and meeting aggressive schedules.

Summary

Design, verification, and optimizable processor IP can help streamline the design process for a variety of mobile applications. With the right IP, you can be assured that your design will comply with the specifications of key mobile protocols; meet power, performance, and area requirements; and be completed on schedule. The time-to-market benefits, in particular, are essential given the short market windows of consumer goods. Cadence's broad portfolio includes silicon-proven IP as well as tools, methodologies, and high-end services that address design and verification challenges covering mobile SoCs all the way up to entire mobile systems.

For More Information

Learn more about Cadence design IP here: <http://ip.cadence.com/ipportfolio/ip-portfolio-overview>

Learn more about Cadence verification IP here: <http://ip.cadence.com/ipportfolio/verification-ip>

Learn more about Cadence Tensilica IP here: <http://ip.cadence.com/ipportfolio/tensilica-ip>



Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud and connectivity applications. www.cadence.com