DESIGN IP BROCHURE

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# Initiator Controller IP for MIPI SoundWire

## Overview

Today's leading-edge mobile devices provide increasingly integrated functionality that enables growing volumes of content and video, more ways to control and interact, and longer battery life. The MIPI Alliance defines semiconductor standards for mobile devices that support growing complexity and reduced device form factor.

The Cadence® IP Family for MIPI® Protocols delivers area-optimized interface IP with the low power and high performance required for today's leading-edge devices. One member of this family is the Cadence Initiator Controller IP for MIPI SoundWire℠ v1.2, providing low-cost, low-power connectivity for audio data transport and control.

Developed by experienced teams with industry-leading domain expertise and extensively validated with multiple hardware platforms. The Controller IP is engineered to quickly and easily integrate with other MIPI compliant IP.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, memory, analog, and system and peripheral IP..

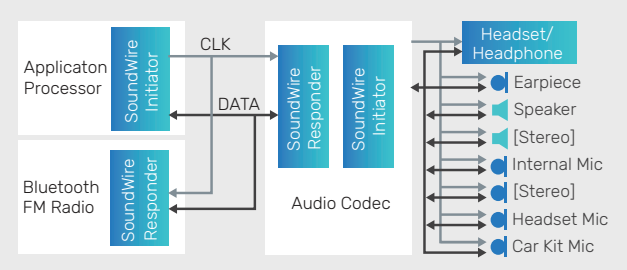


*Figure 1: Example system-level block diagram*

## Benefits

- **Full-featured and highly configurable IP core that is area-optimized for each application**
- **Complete solution—complementary responder also available**
- **Verified in FPGA, silicon-proven**

## Product Details

The Controller IP is designed to provide low-cost, low-power connectivity for audio data transport and control. The SoundWire interface is utilized to provide two types of connectivity. The first carries PCM audio data between a mobile application processor and a standalone audio codec or Bluetooth/FM radio controller. The second type carries PDM audio between the audio codec and MEMS microphone or speaker amplifiers.

## Key Features

- MIPI-compliant initiator controller with multi-lane capability
- Isochronous, TX- or RX-controlled, or fully asynchronous transport
- Configurable port, FIFO, and interface features
- Bus command ownership - BREQ/BREL handshake
- Multi-entry command FIFO for READ/WRITE/PING commands
- Automatic PING generation
- Arm® AMBA® AHB-Lite interface for control register access
- Bi-directional FIFO-based physical data ports for low-latency audio
- Support for Bulk Register Access (BRA) and Bulk Payload Transport (BPT)
- Flexible frame structure

## Register and Command/Response FIFO Access

The control registers can be accessed from a 32-bit AHB-Lite client interface. All registers are mapped to host memory space. Certain timing critical registers are banked to allow synchronous switching without interruption to data streams. The initiator controller also deploys two 32-bit command FIFOs for command issuance (TX) and status tracking (RX). They are accessible through the AHB interface or direct command/response to be attached to an external DMA engine.

## Control Port

The control port supports READ/WRITE/PING commands generation. It also generates synchronization patters that allow responder controllers to synchronize to the bus. The control port controls the bus release mechanism as well as monitoring the status of all devices that are attached to the bus and rises an interrupt in case of status change.

## Data Port

The initiator controller supports configurable numbers (1 to 32) of physical data interface (PDI); each PDI can be configured as TX, RX or bidirectional. The PDI FIFO has configurable width from 1 to 32 bits, and depth of 4 to 32 entries, synchronous or asynchronous.

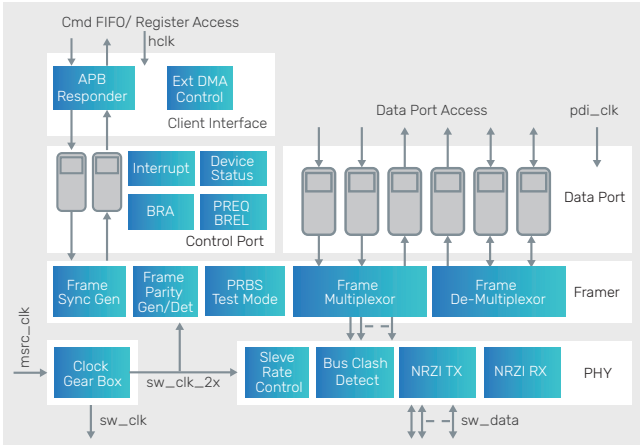


*Figure 2: IP-level block diagram*

## Frame Transport

The initiator controller supports isochronous, TX-controlled, RX controlled, and fully asynchronous transport modes and standard-based frame parameters: offset and sub-frame offset, Hstart and Hstop, sample interval, BlockPackingMode, BlockGroupCount, and LaneSelect.

## Digital PHY Interface

The Controller IP provides a standard interface to the external PHY module with data, data enable, bus keeper enable signals, and slew rate control output. It also provides initialization and calibration logic for training the DQS alignment for each data slice.

## Related Products

- Responder Controller IP for MIPI SoundWire 1.2
- Tensilica® HiFi DSP for Audio
- Manager Controller IP for MIPI SLIMbus®
- Device Controller IP for MIPI SLIMbus
- Design IP for I2S Single Chanel (I2S-SC) and Multi Channel (I2S-MC) Bus Controller
- Controller IP for Sony/Philips Digital Interface Format (S/PDIF)

## Deliverables

- Documentation—implementation specification, user guide, release history
- Clean, readable, synthesizable Verilog RTL
- Synthesis scripts
- Sample verification testbench with integrated BFM, monitors, and sanity tests

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