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Shorting Via Arrays for the Elimination of Package Resonance to Reduce Power Supply Noise in Multi-layered Area-Array IC Packages

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Abstract

This paper presents full-wave electromagnetic field simulations on the effects of shorting via arrays for the reduction of power and ground noise in IC packages. Properties of internal resonance in multi-layered packages are studied. Effects of area-array power and ground vias of different densities are evaluated by examining the input impedances of the package power supply. It is shown that, by properly selecting the density of shorting via arrays, package resonance can be removed from DC to multi-gigahertz frequency range.

I. Introduction

As microprocessor and ASIC power supply voltages are headed to 2.0V and below, and clock frequencies go up to 600MHz and above, the power distribution system of IC packages is becoming an increasingly important design challenge [1]. In high-end flip-chip and ball-grid-array (BGA) packages, multiple power and ground planes are often used to keep power supply noise low. Vias are used to connect power planes at multiple locations, and similarly, ground planes are connected through a number of vias. An important design issue is, for a given power supply noise margin, how to determine the number of power and ground planes, and the number and the locations of power and ground vias.

Electrical performances of power supply systems have often been characterized by effective inductors. The effective inductor model can be used to estimate power supply noise at low frequencies. For high-end packages, the frequency range of interest is from DC to a few gigahertzes. Within this frequency range, there can be several package resonant frequencies, and the effective inductor model may become totally invalid. Accurate characterization of power supply systems necessitates electromagnetic field simulations to take into account various electromagnetic interactions in packages.

II. Fast Electromagnetic Field Simulation for IC Packages

An entire IC package structure often contains multiple metal planes, and hundreds to thousands of vias and traces. General-purpose three-dimensional electro-magnetic tools are at present still impractical to handle entire package structures of that complexity. However, since the separation between metal planes (tens to hundreds of micrometers) is typically several orders of magnitude smaller than the shortest wavelength (several centimeters in digital applications) of interest, the modeling of electromagnetic fields between metal planes can be greatly simplified. With the absence of signal traces between metal planes, the electromagnetic fields between planes are the parallel-plate mode of fields. Propagation of the parallel-plate mode fields can be modeled through distributed capacitor and inductor meshes [2-3], or equivalently through transmission line meshes [4]. In [2-4], because the large number of capacitors and inductors, or transmission lines, are handled by conventional circuit solvers, the simulation time can be quite long even for modestly dense meshes. It has been shown that the simulation of the propagation of parallel-plate mode fields can be orders of magnitude faster if the fields are computed through the finite-difference solution of the corresponding partial deferential equations, instead of through distributed capacitor and inductor, or transmission line meshes.

With the presence of signal traces between metal planes, the electromagnetic fields between planes can be viewed as the superposition of the parallel-plate mode and the strip-line mode fields. Techniques have been developed to automatically take into account interactions between two modes of fields, and to link the electromagnetic field solver with circuit solvers [5-7]. Some hardware measurement verifications of the techniques were reported in [8]. The simulation results of this paper are computed by SPEED97 [9], which is a recently released commercial software based on the techniques in [5-7].

III. Package Input Impedance and Internal Resonance

For a given switching current at terminals of a power supply system, the voltage fluctuation at the terminals is simply the current times the input impedance of the power supply system. To ensure low power supply noise, the input impedance of the power supply system should be kept low from DC to several times the clock frequency [1]. Power and ground planes usually provide low impedance for the power supply system. However, due to reflections from edges of metal planes, resonance can happen inside packages and large input impedance values will appear around resonant frequencies.

Configurations of examples for the illustration of package resonance are shown in Fig. 1 and 2. The metal planes are of size 6.56 cm by 6.56 cm. The dielectric constant of the medium between metal planes is chosen to be 9. The separation between metal planes is 300 μ m. The radius of vias is 50 μ m.

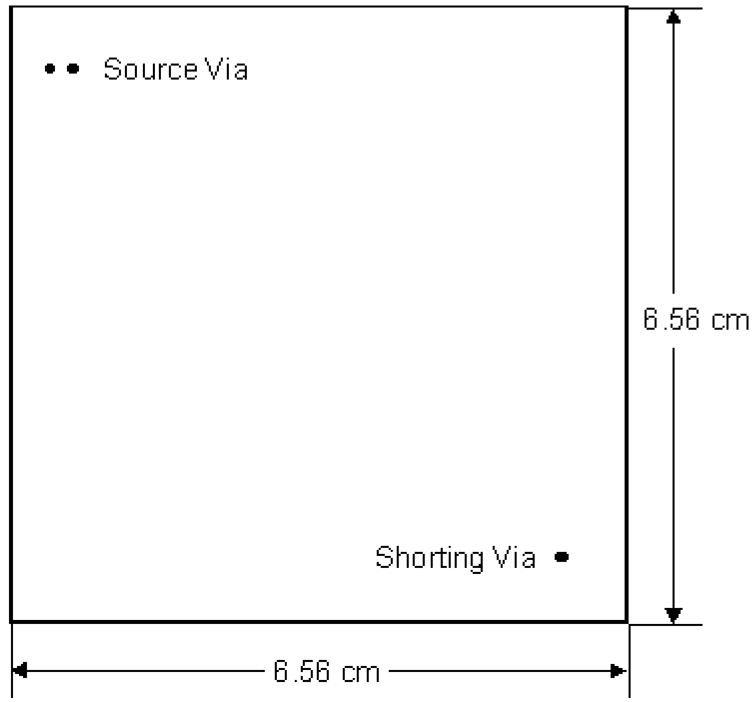


Fig. 1 Top view of metal planes

The frequency-dependent input impedance is calculated as follows. Connect a source circuit to a pair of vias near the upper left corner of metal planes, as shown in Fig. 1. The source circuit contains a resistor of 2 Ohms in series with a voltage source. The waveform of the voltage source is a Gaussian pulse of 200 ps pulse width. The spectrum of the Gaussian pulse is from DC to about 3GHz. The 2 Ohm resistor is to provide damping to the time-domain response. The time-domain voltage across the source circuit and the current flowing through the via connected to the source circuit are recorded during the time-domain simulation. After the time-domain simulation is completed, the input impedance is obtained by the ratio of the Fourier transform of the voltage across the source circuit and the Fourier transform of the current flowing through the source via.

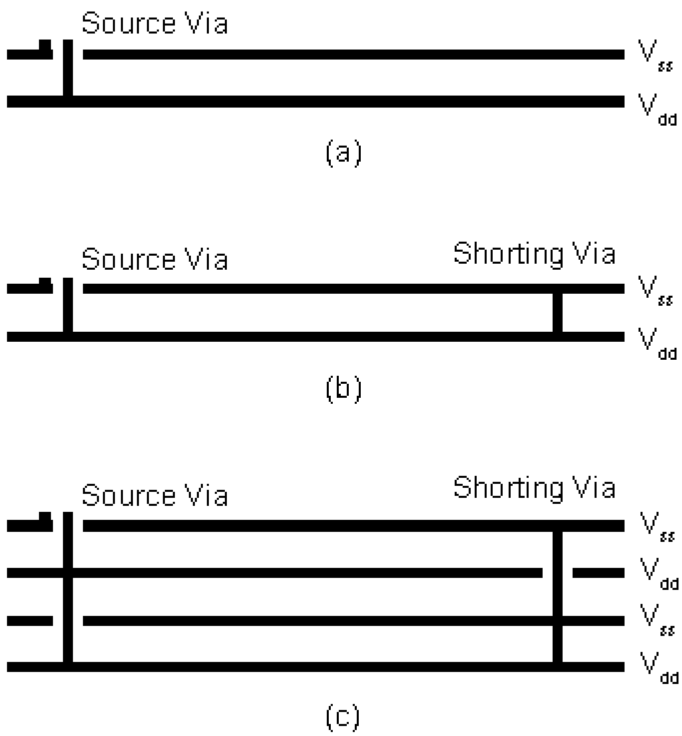


Fig. 2 Side view the metal plane configuration

(a) two parallel planes, (b) two parallel planes with a shorting via, (c) four parallel planes with shorting vias

For the two parallel metal planes shown in Fig. 2(a), resonant frequencies can be found analytically as

$$f_{mn} = \frac{1}{2a\sqrt{\mu_0 \varepsilon_0 \varepsilon_r}} \sqrt{\mathrm{m}^2 + n^2}\ (\mathrm{m, n} = 0, 1, 2, \ldots)$$

(1)

where a = 6.56 cm, ε_r = 9. The first several resonant frequencies are listed in the following table:

Table 1. Resonant frequencies in GHz of the two parallel metal planes of Fig. 2(a)

m, n	0	1	2	3
0		0.7617	1.5233	2.2850
1	0.7617	1.0772	1.7031	2.4086
2	1.5233	1.7031	2.1543	2.7462
3	2.2850	2.4086	2.7462	3.2315

Numerically computed input impedances as a function of frequency are displayed in Fig. 3. It can be seen from the solid line of Fig.3 that, for the parallel metal plane structure of Fig. 2(a), the resonant frequencies revealed in the numerically computed input impedance match very well with those obtained analytically from (1). The input impedances in the above and following examples are observed at the corner of metal planes. This is because inside metal planes, certain resonant frequencies may not be observed. For example, at the center of the metal planes, resonant frequencies at only 1.52GHz and 2.15GHz in Table 1 can be observed.

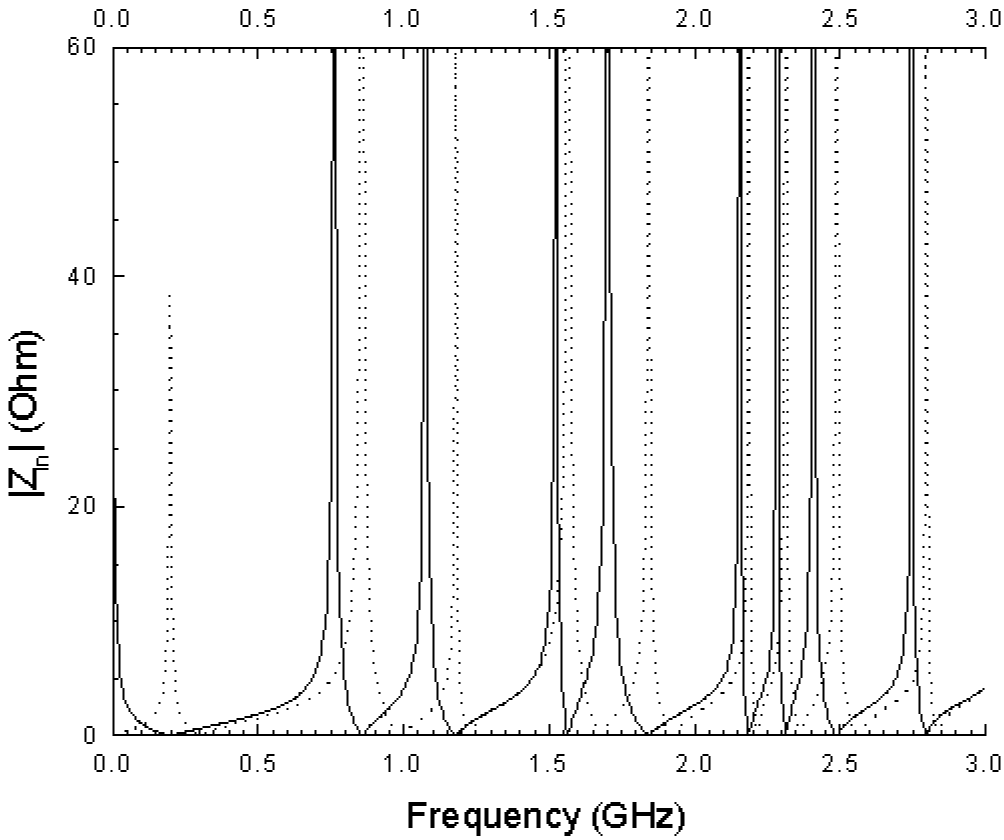


Fig. 3 Input impedance of parallel metal planes. Solid line: two metal planes shown in Fig. 2(a). Dot line: two metal planes with a shorting via shown in Fig. 2(b)

The first resonant frequency of the parallel-plate structure is at 761.7MHz. However, as the power and ground planes are connected to a low-impedance power supply, the first resonant frequency can become much lower. Fig. 1 and Fig 2(b) show that the power and ground planes are connected to an external power supply near the lower right corner of the metal planes. The impedance of the external power supply is assumed to be zero, so that the connection to the external power supply is modeled by a via connecting the two metal planes. The input impedance of the structure in Fig. 2(b) is shown as the dot line in Fig.3. It can be seen that, with the addition of that shorting via, resonant frequencies are shifted from those predicted by (1). But more importantly, there is an addition of a resonant frequency as low as 195MHz. This resonance, which has also been observed in [10], is due to the quarter-wavelength resonance between the shorting via at the lower right corner and the open-circuit metal plane edges at the upper left corner. When two more planes are added, and when the planes are connected as shown in Fig. 2(c), the quarter-wavelength resonance path becomes longer than that in Fig. 2(b), and the first resonant frequency now appears at 70MHz as displayed in Fig. 4.

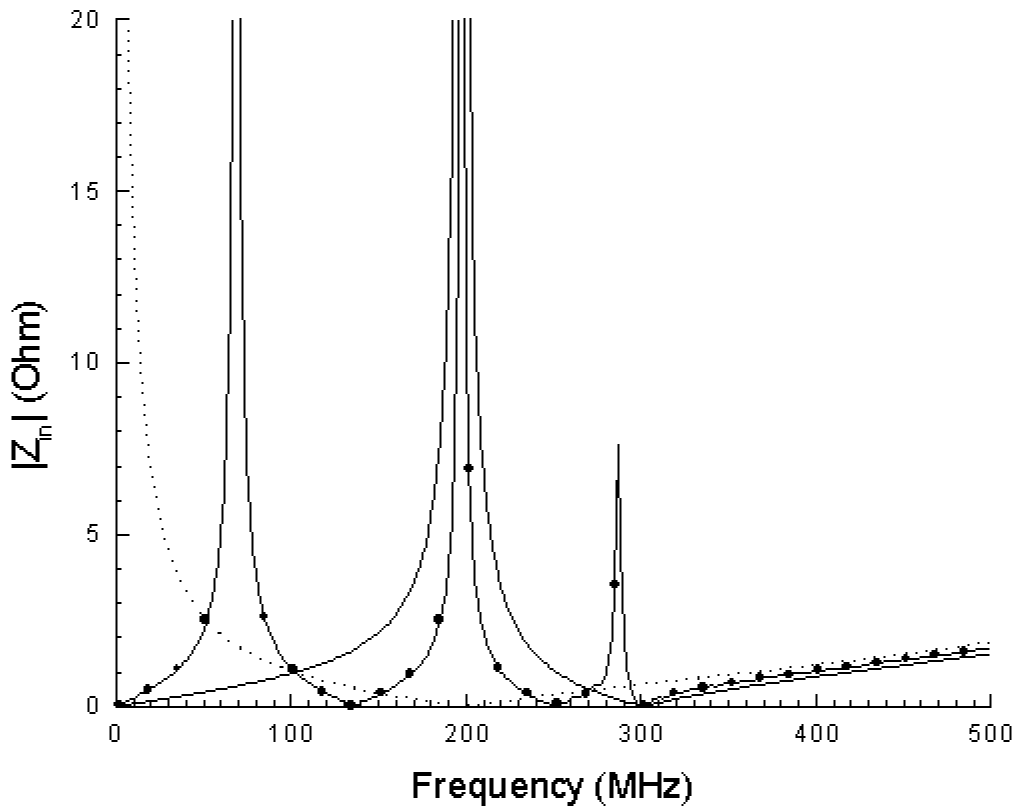


Fig. 4 Input impedances of multiple power and ground planes. Dot line: two metal planes shown in Fig. 2(a). Solid line: two metal planes with a shorting via shown in Fig. 2(b). Solid line with circles: four metal planes with shorting vias shown in Fig. 2 (c).

The above examples illustrate that in multi-layered IC packages, resonance inside package structures can lead to resonant frequencies well within the frequency range of interest of most high-end digital applications.

IV. Effects of Shorting Via Arrays

To maintain low input impedance of power supply systems, the resonances within the frequency range of interest have to be eliminated. It will be shown that low-frequency resonances can be effectively removed by placing an array of vias connecting the power and ground planes.

In the following tests, to concentrate on the study of properties of IC packages, the external power supply connected to the package power supply system is assumed ideal. That is, the input impedance of the external power supply is assumed to be zero. The DC voltage source of the external power supply can also be removed in analysis since it does not affect the AC properties of the package power supply system.

The package power supply system studied here has three metal planes as shown in Fig. 5. The horizontal dimensions of the metal planes are the same as those of Fig.1. Vias connected to the external power supply are terminated at the bottom metal plane to model the ideal external power supply. The Vdd vias connected to power planes and the Vss vias connected to ground planes are arranged in the way shown in Fig. 6. The input impedance is observed at the lower left corner (0.02 cm, 0.02 cm).

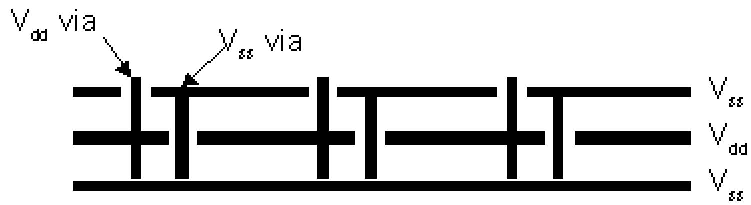
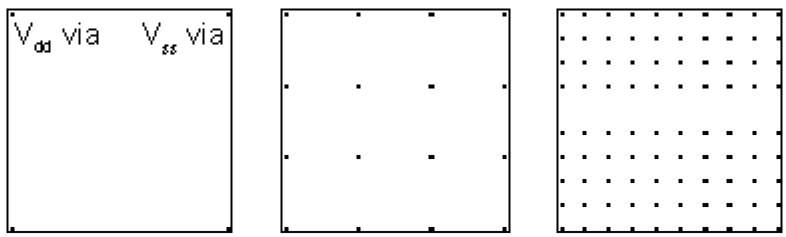


Fig. 5 Metal planes of a package power supply system



(a) (b) (c)

Fig. 6 Power and ground via arrangement.

(a) 2 by 2 via array. (b) 4 by 4 via array. (c) 10 by 10 via array.

The input impedances of the package power supply system due to shorting via arrays of different densities are shown in Fig. 7. It can be found from Fig. 7 that, as the via density becomes larger, the lowest package resonant frequency moves higher. The lowest resonant frequencies for 2 x 2, 4 x 4 and 10 x 10 via arrays are at 110MHz, 335MHz and 1.075GHz respectively. When the density of via array is 28 by 28 or higher, there is no resonance in the frequency range of DC to 3GHz.

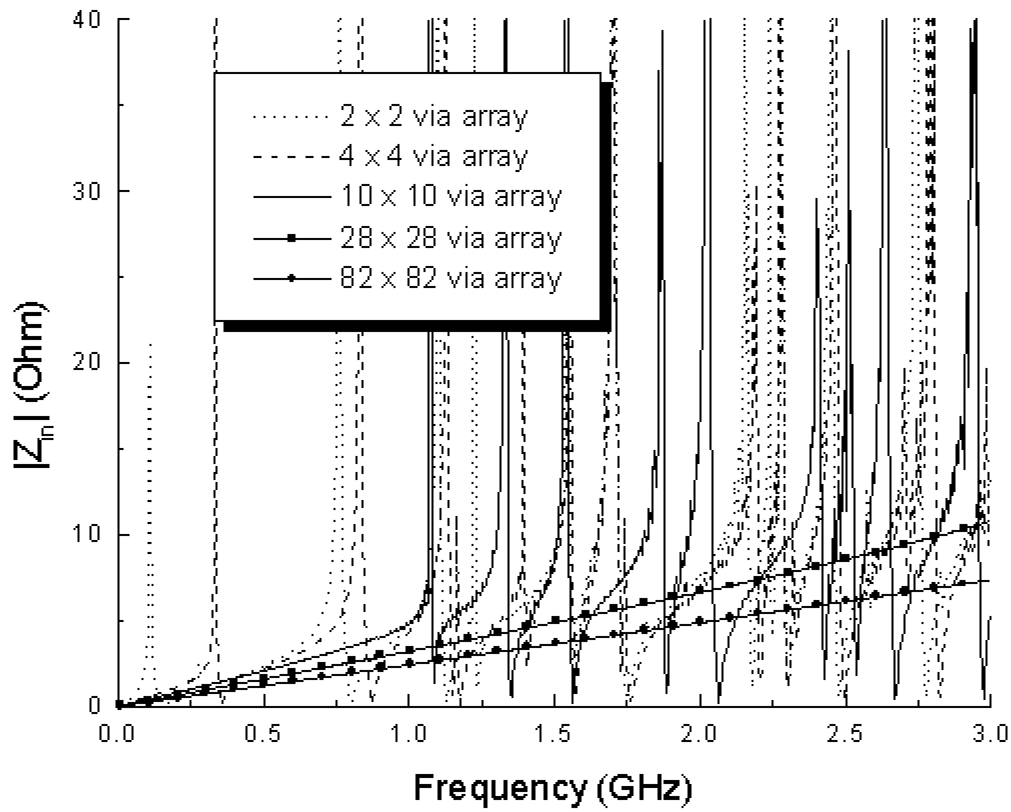


Fig. 7 Input impedances of different via array densities

The above example shows that, by properly selecting the density of shorting via arrays, package resonance can be completely removed from DC to multi-gigahertz frequency range.

References

1. Larry Smith, "Packaging and Power Distribution Design Considerations for Sun Microsystems Desktop Workstation," IEEE 6th Topical Meeting on Electrical Performance of Electronic Packaging, Conference Proceedings, pp. 19-22, Oct. 27-29, 1997, San Jose, CA.
2. H. Hashemi and D. Herrel, "Power Distribution Fidelity of Wirebond Compared to Flip Chip Devices in Grid Array Packages," IEEE Trans. Components, Hybrids and Mfg. Tech., Part B, vol. 20, No. 3, pp. 272-278, Aug. 1995.
3. J. Yook, L. Katehi, K. Sakellah, R. Martin, L. Huang, and T. Schreyer, "Application of System-Level EM Modeling to High-Speed Digital IC Packages and PCB's," IEEE Trans. Microwave Theory Tech., vol. 45, No. 10, pp. 1847-1856, Oct. 1997.
4. K. Lee and A. Barber, "Modeling and Analysis of Multichip Module Power Supply Planes," IEEE Trans. Components, Hybrids and Mfg. Tech., Part B, vol. 18, No. 4, pp. 628-639, Nov. 1995.
5. J. Fang, Y. Chen, Z. Wu and D. Xue, "Model of Interaction Between Signal Vias and Metal Planes in Electronics Packaging," *Proceedings of IEEE Third Topical Meeting on Electrical Performance of Electronic Packaging,* Monterey, CA, Nov. 2-4, 1994, pp. 211-214.
6. Y. Chen, Z. Chen, Z. Wu, D. Xue and J. Fang, "A New Approach to Signal Integrity Analysis of High-Speed Packaging," *Proceedings of IEEE Fourth Topical Meeting on Electrical Performance of Electronic Packaging,* Portland, Oregon, Oct. 2-4, 1995, pp. 235-238.
7. J. Fang, Z. Chen, Y. Chen, D. Xue and J. Zhao, "Integrated Electromagnetic and Circuit Simulation for Signal Integrity Analysis of High-Speed Electronic Packages," Proceedings of 1997 Government Microcircuit Applications Conference, pp. 347-350, March 10-13, 1997, Las Vegas, Nevada.

8. S. Rosser, M. Kerr, C. S. Chang, J. Fang, Z. Chen and Y. Chen, "Measurement and Simulation of Simultaneous Switching Noise in the Multi-Reference Plane Package," Proceedings of *46th Electronic Components and Technology Conference*, Orlando, FL, May 28-31, 1996, pp. 660-670.

9. Information on SPEED97, which is produced by SIGRITY, can be found from www.sigrity.com

10. A. R. Djordjevic and T. K. Sarkar, "An Investigation of Delta-I Noise on Integrated Circuits," IEEE Trans. Electromagn. Compat., vol. 35, No. 2, pp. 134-147, May 1993.