Power Integrity

Dr. Eric Kuo  Eric_Kuo@gemteks.com
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Root Cause of PI

\[ \Delta V = \text{Lv} \frac{\Delta I}{\Delta t} \]

\[ \Delta V = \text{Lg} \frac{\Delta I}{\Delta t} \]

CPU/DSP/Switching chip are the class of low-voltage high current applications
Z-Profile of PWR/GND Planes

Value goes to infinity at DC

\[ V(f) = I(f) \times Z(f) = I \times Z_{DC} + I_1 Z_{PDN@HF} \]

Vdd \ (+/-5\% Vdd)

Capacitive behavior before resonance

@ DC \ (\rightarrow \text{Open})

@ HF \ (\rightarrow \text{Behave as capacitive})

\[ Z_{PDN} \]
Resonance/Anti-resonance

\[ Z = \frac{V}{I} \]

- Resonance → \( Z \) approaches to zero
  - No matter how large the current is, there is no voltage drop
  - No reliability issue

- Anti-resonance → \( Z \) approaches to infinity
  - Even very small current will drive a huge voltage drop
  - Reliability issue
Equivalent Ckt of PDN
From the data sheet of the switching circuit, the consumed power and applied voltage are usually given, hence

\[ I_{\text{max}} = \frac{P}{V} \]

The average current is assumed to be 50% of the maximum current, then

\[ Z_T = \frac{V_{dd} \times \text{ripple}}{50\% \times I_{\text{max}}} \]
Bypass/Decoupling Capacitors

- Switching circuit requires current to charge the load
- If the output impedance is too high, then VRM is unable to respond well (VRM output impedance exceeds the desired impedance)
- External capacitors store charge. They bypass the VRM and supply the current to the switching circuit
- The bypass capacitors are also called decoupling capacitors (decouple the VRM from the switching circuit)
ESR & ESL of the Decoupling Capacitor

Equivalent circuit of decoupling capacitor
Z-Profile of Decoupling Capacitor

- **Shunt Model**: Terminated with 50Ω
- **Series Model**: Terminated with GND
- **Ideal Cap**: Capacitive -20dB/decade, Inductive +20dB/decade

freq, Hz

mag(Z(1,1))

mag(Z(2,2))

mag(Z(3,3))

ESR
Decoupling Capacitors

- Decouple the VRM from the switching circuit
  - Provides a low impedance path
Ultra Low Impedance Measurement

- 1-Port Measurement

\[ Z = \left( \frac{1 + S_{11}}{1 - S_{11}} \right) Z_0 \]

Impedance of PDN is usually much smaller than 50Ω
\[ \Rightarrow |S_{11}| \sim 1 \]
It makes the Z cannot be slow enough

- 2-Port Measurement

\[ Z_{11} = 25 \times \left( \frac{S_{12}}{1 - S_{12}} \right) \]
Calculated Z-Profile

Bare board

\[ C = \varepsilon_0 \varepsilon_r \frac{A}{d} = 8.854 \times 10^{-12} \text{ F/m} \times 4.2 \times 0.05^2 \text{ m}^2 / (10/40 \times 10^{-3} \text{ m}) = 372 \text{ pF} \]

At 300 kHz, \( Z_c = \frac{1}{(\omega C)} = 1.426 \times 10^3 \Omega \)

De-Cap: 1uF

At 300 kHz, \( Z_c = \frac{1}{(\omega C)} = 0.5305 \Omega \)
Measurement: Bare Board

Simulation w/ transmission line effect
Measurement: Bare Board De-embedded

TB-074_V00-0521_noDecap.spd

D:\Sigirty_Course\David_TestBoard\C16_bare_Deembedded.s1p - Z1[1,1] - Z(1:1::, 1:1::)

SIMULATION - Z0[1,1] - Z(1:Port1::VCC_LAYER3, 1:Port1::VCC_LAYER3)
Measurement: Board W/ Decap

Simulation w/ transmission line effect
Measurement: Board W/ Decap De-embedded

Z Amplitude (Ohm)

TB-074_V00-0521.spd

Frequency (GHz)

D:\Sigirty_Course\David_TestBoard\C16_Deembedded.s1p - Z4[1,1] - Z[1:1::, 1:1::]
SIMULATION - Z0[1,1] - Z[1:Port1:: VCC_LAYER3, 1:Port1:: VCC_LAYER3]
Example 2: DDR3-1600
Target Impedance Estimation

- In data sheet, the $I_{\text{max}} = 210\text{mA}$
- The swing is from 1.4V to 1.6V (ripple is +/- 6.67%)
- Hence the target impedance can be calculated as

\[
Z_T = \frac{V_{dd} \times \text{ripple}}{50\% \times I_{\text{max}}} = \frac{1.5 \times 0.067}{0.5 \times 0.21} = 0.957\Omega
\]
Correlation
Ultra Low Impedance Measurement

2-Port measurement to capture the ultra low impedance
\[ Z = 25 \times \left| \frac{S_{21}}{1 - S_{21}} \right| \]
ESL & ESR Effect

freq, Hz

ADS_Decap
Meas_Decap
Sigrity_Decap

1E-2
1E-1
1
1E1
1E2
1E6 1E7 1E8 1E9 4E9
Z-Profile @ U101, U201, and U204

400 MHz
DQ1 Only: Write

- **DQ1**
  - **W/ Decap**
  - **W/O Decap**

- **VDD @ RAM**
  - **W/ Decap**
  - **W/O Decap**
All DQ: Write

VDD swing from 1.42 ~ 1.55, within the spec (1.5 +/- 6.67%)
All DQ: Read

VDD swing from 1.45~ 1.55, within the spec (1.5 +/- 6.67%)
Conclusions

• Target impedance is the main parameter to design the power plane
• Ultra-low impedance measurement and proper embedded technique should be applied to obtain the good correlation
• Sigrity PowerSI and SystemSI provides an user-friendly workflow to speed up the design flow
References


• Agilent ultra-low impedance measurements using 2-port measurement, application note, 2007