

# A Fast Evaluation of Power Delivery System Input Impedance of Printed Circuit Boards with Decoupling Capacitors

Jin Zhao ([jzhao@sigrity.com](mailto:jzhao@sigrity.com))  
Sigrity Inc., Santa Clara, CA 95051  
Om P. Mandhana ([Om.Mandhana@freescale.com](mailto:Om.Mandhana@freescale.com))  
Freescale Semiconductor, Austin, TX 78729

## Abstract

A fast power delivery system input impedance evaluation methodology for printed circuit board decoupling capacitor placement study is presented in this paper. The methodology is based on electrical network admittance matrix properties. The admittance matrix methodology described in this paper is rigorously validated by comparing the decoupling capacitor placement evaluation of a real printed circuit board by both impedance matrix and results from commercial electromagnetic field software.

## Introduction

In order to ensure a noise-free, stable power delivery to the electronic devices (IC chips) mounted on a printed circuit board through packages, hundreds of different types of decoupling capacitors are placed on board. Efficiently selecting and placing decoupling capacitors on a printed circuit board for cost effective design of the power delivery system is a critical task for power integrity engineers [1~5].

Traditionally, printed circuit board power delivery system has been represented as multi-stage lumped circuit. However, as frequency increases, the lumped circuit models suffer from the inaccuracy because the board dimension becomes comparable with the wavelength of the frequency range. The wave propagation effects must be accounted in the analysis and design of a power delivery system.

There are several critical issues related to the printed circuit board decoupling capacitor placement, such as 1) optimal type of a decoupling capacitor; and 2) overall cost of different types of the decoupling capacitors. In order to solve these issues, a fast evaluation of power delivery system input impedance is necessary.

In general, for a post-layout performance optimization of the input impedance or for a new product design based on old designs, the decoupling capacitors mounting locations are already defined on the printed circuit boards. Therefore, in this paper, it is assumed that all the decoupling capacitors mounting locations on the board are pre-defined. The network parameters such as impedance matrix for the power delivery system can be obtained from the frequency domain simulation results using a commercial electromagnetic field solver [6]. The input impedance for different number and types of decoupling capacitors at locations of interest can be obtained from these impedance matrix parameters. It is important to note that for simulation using such field solvers, electrical ports are defined at those pre-defined locations of the decoupling capacitors or at any other locations at which the power and ground input impedance are interested. The input impedance for different number and types of decoupling capacitors on the printed circuit board can also be easily computed by combining the impedance matrix of the power delivery system obtained from the field solver without any decoupling capacitor on the board and the impedance matrix corresponding to the number and types of decoupling capacitors mounted on the board. However, such iterative computations of the power delivery input impedance becomes time consuming for large number and types of decoupling capacitors placed on board. Based on the admittance matrix properties, a fast and simple input impedance computation methodology for such type of situations is introduced in this paper. The input impedance computational methodology described in this paper is applied to a real printed circuit board and is validated by comparing the input impedance with that obtained directly from the electromagnetic field solver.

## Principle

Consider a post-layout printed circuit board as shown in Fig. 1, which consists of several locations for IC devices, where the input impedance between power and ground is of interest, voltage regulator modules and decoupling capacitors at pre-defined locations. By defining ports at decoupling capacitor locations and at other critical component locations on the board, an impedance matrix for the power delivery system can be obtained by using a commercially available field solver [6], as:

$$\begin{bmatrix} V_1 & \dots & V_n & V_{n+1} & \dots & V_{n+m} \end{bmatrix}' = [Z]_{(n+m) \times (n+m)} \begin{bmatrix} I_1 & \dots & I_n & I_{n+1} & \dots & I_{n+m} \end{bmatrix}' \quad (1)$$

where  $V_1 \dots V_n$  and  $I_1 \dots I_n$  are the voltages and currents respectively at the locations of the components at which the ports 1 to n are defined on the board. Similarly,  $V_{n+1} \dots V_{n+m}$  and  $I_{n+1} \dots I_{n+m}$  are the voltages and currents respectively at the decoupling capacitor locations where ports n+1 to n+m are defined. Equation (1) can be expressed in the blocked matrix form, as:

$$\begin{bmatrix} \tilde{V}_1 \\ \tilde{V}_2 \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{11} & \tilde{Z}_{12} \\ \tilde{Z}_{21} & \tilde{Z}_{22} \end{bmatrix} \begin{bmatrix} \tilde{I}_1 \\ \tilde{I}_2 \end{bmatrix} \quad (2)$$

where,  $\tilde{V}_2$  and  $\tilde{I}_2$  are the voltage and current vectors respectively, corresponding to ports defined at the decoupling capacitor locations. Similarly,  $\tilde{V}_1$  and  $\tilde{I}_1$  represent the voltage and current vectors respectively, corresponding to ports defined at all other locations of interest. Also,  $\tilde{Z}_{11}$  and  $\tilde{Z}_{22}$  are defined as the blocked self impedance matrices and  $\tilde{Z}_{12}$  and  $\tilde{Z}_{21}$  are defined as the blocked transfer impedance matrices relating the voltages and currents at the port locations on the printed circuit board of Fig. 1.

Notice that the voltage and current relation for the decoupling capacitors on the board, can be expressed in the matrix form as

$$\tilde{V}_2 = \text{diag}(-Z_{\text{decap}})_{m \times m} \tilde{I}_2 \quad (3)$$

By combining equations (2) and (3) a new input impedance matrix  $[Z]_{n \times n}$ , of reduced order n, can be obtained as

$$[Z]_{n \times n} = \tilde{Z}_{11} - \tilde{Z}_{12} (\text{diag}(Z_{\text{decap}})_{m \times m} + \tilde{Z}_{22})^{-1} \tilde{Z}_{21} \quad (4)$$

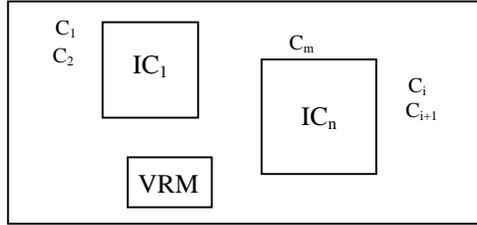


Figure 1. A printed circuit board with several ICs, VRM, and many decoupling capacitors mounted

However, such input impedance computation becomes very time-consuming as the number of decoupling capacitors placed on board increases. The input impedance computation process using equation (4) involves large matrix inverse with several large matrix multiplications at every frequency point. Also, as the impedance of a decoupling capacitor is embedded into the matrix operations, it becomes difficult to select a decoupling capacitor of appropriate capacitance, ESR (equivalent series resistance) and ESL (equivalent series inductance).

In order to alleviate these problems, a fast and simple computational methodology for power delivery systems, based on the properties of electrical network admittance matrix is described next. The basic idea of the methodology can be illustrated using Fig. 2.

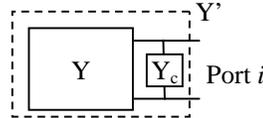


Figure 2. Illustration on admittance utilization

In Fig. 2, Y represents the power ground admittance matrix for the printed circuit board without any decoupling capacitors mounted and  $Y_c$  is the admittance of a decoupling capacitor mounted at Port  $i$ . From the admittance matrix property, the resultant power ground admittance matrix  $Y'$  can be calculated by adding  $Y_c$  to the diagonal matrix Y, such that,

$$Y' = Y + \text{diag} \left\{ \begin{matrix} 0 & \text{others} \\ Y_c & \text{ith entry} \end{matrix} \right\} \quad (5)$$

If there are multiple decoupling capacitors mounted at other ports, then the diagonal elements of matrix  $Y_c$  will have multiple non-zero entries corresponding to the admittance of the decoupling capacitor at the location of the ports. Therefore, equation (5), in matrix form can be expressed as

$$Y' = Y + \begin{bmatrix} 0 & & & & \\ & Y_{c1} & & & \\ & & Y_{c2} & & \\ & & & \ddots & \\ & & & & Y_{cm} \end{bmatrix} \quad (6)$$

If there is no decoupling capacitor connected at the port location, the corresponding  $Y_c$  matrix element is 0.

Therefore, the procedure for the fast power ground input impedance computation could be described as follows.

1. For a given printed circuit board, an admittance matrix can be obtained using a commercially available field solver. Next, by rearranging the entries of the admittance matrix, a blocked admittance matrix similar to equation (2) can be generated as,

$$\begin{bmatrix} \tilde{I}_1 \\ \tilde{I}_2 \end{bmatrix} = \begin{bmatrix} \tilde{Y}_{11} & \tilde{Y}_{12} \\ \tilde{Y}_{21} & \tilde{Y}_{22} \end{bmatrix} \begin{bmatrix} \tilde{V}_1 \\ \tilde{V}_2 \end{bmatrix} \quad (7)$$

2. A decoupling capacitor admittance matrix  $\tilde{Y}_C$  can be generated as a diagonal matrix. If at port  $i$ , a decoupling capacitor is connected, then the  $i$ th entry of the matrix  $\tilde{Y}_C$  is  $Y_{ci}$ , where  $Y_{ci}$  denotes the admittance of the decoupling capacitor connected at the port location on board. Similarly, the  $i$ th entry of the matrix  $\tilde{Y}_C$  is 0, corresponding to no decoupling capacitor connected at the  $i$ th port location.
3. The resultant power and ground admittance matrix can be calculated as

$$[Y] = \begin{bmatrix} \tilde{Y}_{11} & \tilde{Y}_{12} \\ \tilde{Y}_{21} & \tilde{Y}_{22} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & \tilde{Y}_c \end{bmatrix} \quad (8)$$

4. Finally, the impedance matrix can be obtained from equation (8), as

$$[Z] = [Y]^{-1} \quad (9)$$

The elements  $Z_{ii}$  ( $i = 1 \dots n$ ) of the impedance matrix of equation (9) represent the power ground input impedance at the port locations  $i$  ( $i = 1 \dots n$ ).

### Simulation and Numerical Results

A six-layer, 100 mm by 60 mm printed circuit board, as shown in Fig. (3) is used as an example to illustrate the input impedance computation methodology for a power delivery system described in the previous section. The microprocessor package on the board, where the power ground input impedance is of interest is shown as U17 in the top view of Fig. 3. The voltage regulator module located at the edge connector on the board feeds power to the microprocessor. In this paper, the voltage regulator module is assumed as an ideal voltage source and is modeled as a short circuit for the purpose of frequency domain analysis of the board using the commercially available field solver. There are eight decoupling capacitors (C21~C28), each of 0.022  $\mu$ F, mounted on the topside of the board. Also, mounted on the bottom side of the board, are twenty (C1~C20) decoupling capacitors, each of 0.01  $\mu$ F and eight (C29~C36) decoupling capacitors each of 1.0  $\mu$ F.

The input impedance characteristic of the power delivery system looking from the location of U17 is obtained by two different methods. First, the input impedance is obtained from simulation using a commercial field solver with a single port connected at the location of U17, between all lumped power pins and all lumped ground pins. Figure 4 shows the input impedance characteristics of the board looking from the location of U17, with and without 36 decoupling capacitors on the board.

Next, simulation is performed using the same field solver, with a port connected at each of the 36 decoupling capacitor-mounting locations on the board, and a port between all lumped power pins and all lumped ground pins at location of U17. With 37 ports defined on board, and with no decoupling capacitors, an admittance matrix is obtained from the field solver. Using this admittance matrix of the board, the input impedance matrix for 36 decoupling capacitors mounted on the board is computed from equation (9) described in the last section. For the purpose of comparison, Fig. 5 shows two input impedance magnitude plots generated by these two methods. One can see that the two curves shown in Fig. 5 are identical.

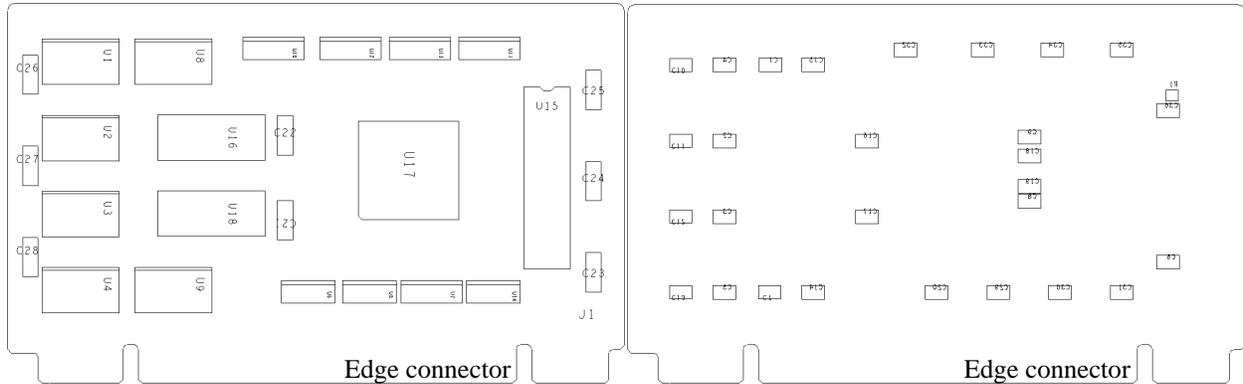


Figure 3. Top (left) and bottom (right) view of the printed circuit board used for numerical testing

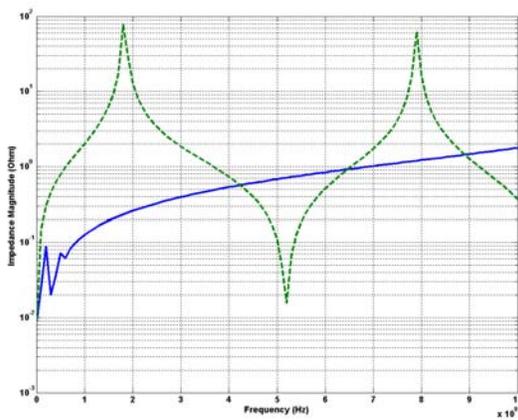


Figure 4. Input impedance with and without decoupling capacitors mounted on the board

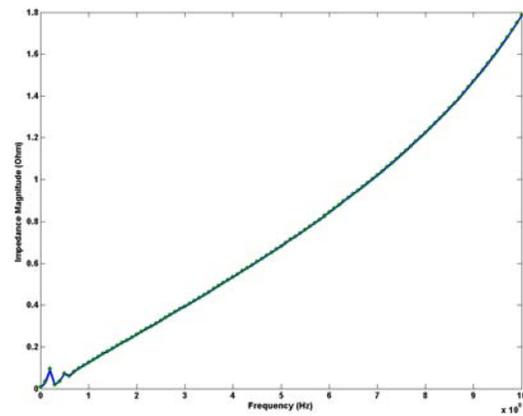


Figure 5. Input impedance obtained from commercial software, and admittance approaches

## Conclusion

A fast power ground input impedance evaluation methodology for the printed circuit board with decoupling capacitor placement study is introduced in this paper. Simulation using a commercially available field solver and numerical computation of input impedance using the admittance matrix approach shows that the methodology presented in this paper can accurately estimate the power and ground input impedance up to gigahertz frequency range, which is typically high enough for board level power delivery system with decoupling capacitors.

## Reference

- [1] L. Smith, *et al.*, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," *IEEE Trans. Advanced Packaging*, vol.22, pp. 284-290, Aug. 1999
- [2] D. Herrell, and B. Beker, "Modeling of Power Distribution Systems for High-Performance Microprocessors," *IEEE Trans. Advanced Packaging*, vol.22, pp. 240-248, Aug. 1999
- [3] W. Beyne, C. Yuan, J. Kim, and M. Swaminathan, "Modeling and analysis of Power Distribution Network for Gigabit Applications", Proceedings of the International Symposium on Quality Electronic Design (ISQED'03)
- [4] J. Choi, S. Chun, N. Na, M. Swaminathan and L. Smith, "A Methodology for the Placement and Optimization of Decoupling Capacitors", 13<sup>th</sup> International Conference on VLSI, Jan. 2000
- [5] O. Mandhana, J. Zhao, "Power Delivery System Performance Optimization of a Printed Circuit Board with Multiple Microprocessors," in Proc. 54<sup>th</sup> ECTC, Las Vegas, NV, 2004, pp. 581-588
- [6] PowerSI, [www.sigritty.com](http://www.sigritty.com)