Accurate Modelling of PCIe® 3.0 Analog Buffers

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Agenda

- Problem Statement
- Overview of IBIS-AMI Modeling
- Accurate Modeling of PCIe® SerDes IO for 16Gbps or Higher Speeds
  - Using Parameterized AMI Blocks
  - Using Virtual Reference Design (VRD) Flow for Quick Sign-off
- Conclusion
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Problem Statement

- PCIe 3.0 and other current and future high speed protocols require complex equalization schemes to open the eye at the receiver sampler.
- These equalizers (AGC, CTE, DFE, etc.) interact with each other during adaptation.
- Managing this sequence of events can be challenging.
- Correlation is even more challenging.
Channel Simulation; EQ Basics

**FFE**
- Preemphasis or deemphasis to compensate for channel loss
- Can do precursors and post cursors
- Can optimize for the channel as impulse response is provided in software simulation, else supports backchannel
  - Static, no real adaptation
  - Avoid if pwr is main concern

**Impulse Response**
- Curve based function to boost the incoming signal so that it could be detected at the output
  - Noise also gets boosted

**Channel**

**Auto Gain Control (AGC)**
- Selective boosting at frequency of interest (high freq channel loss cancellation)
  - Better for area/power considerations
  - Noise and xtalk also gets boosted
  - Usually first order filter only

**Continuous Time Eq (CTLE)**
- Feeds back previous bit decisions to cancel post cursor ISI caused by them
  - Can model non-linearity
  - Adaptively tunes tap coefficient
  - Level sensitive
  - Cannot cancel pre-cursor
  - Needs ‘something’ to work with → AGC/CTLE

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Objectives of Equalization

- Maximize SNR
  - Done by reducing the area/spread of the PDF
- Auto DFE figures out the peak and tries to maximize the peak
  - Focus on the center, works better in crosstalk minimization
  - Digitally aware
- CTE follows the DFE
  - Analog (indirectly sharpens IR)
  - Cheap/less power/area
  - Can amplify noise
- VGA amplifies the target to achieve the target
  - Which also amplifies the noise
  - Lower dv_target – the better for noise
    - IF the Rx can detect (Tradeoff)
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AMI > Algorithmic Modeling Interface

- Extension made to IBIS in 2007
  - **Cadence** at the forefront of driving AMI through the standardization process

- Enables executable, software-based, algorithmic models to work together with traditional IBIS circuit models
  - Allows deeper access to on-chip technology/secret sauce

- Enables SerDes adaptive equalization algorithms to be modeled and used during channel simulation
  - Fast, accurate and flexible
Motivation for AMI

- Interoperability: IBIS-AMI allows plug-and-play simulation compatibility between SerDes models from different suppliers, in a standard commercial EDA format.
- IP Protection: Shared Objects (dlls) are compiled. EDA tool communicates with the dll using the standardized API.
- Flexibility: The Model Maker can use any high level programming language (ex C) to describe the eq at both ends.
IBIS-AMI Model Sub-Components

- Circuit part
  - IO buffer stage
  - Voltage swing
  - Parasitics
  - Spice or traditional IBIS format

- Algorithmic part
  - On-chip
  - Equalization functionality
  - DLL + AMI file
APIs in IBIS-AMI Modeling

- **AMI_Init**
  - Initialize filter
  - Setup Data Structures

- **AMI_GetWave**
  - Waveform Processing
  - Clock and Data Recovery

- **AMI_Close**
  - Free memory etc.

- **AMI_Init** for “one-time adaptive EQs”
- **AMI_GetWave** for “real-time adaptive EQs”

Model input parameters

Impulse Response

Continuous waveform

Modified Impulse Response

Equalized waveform

Clock tics
IBIS-AMI and Channel Simulation

Channel Simulator

- Package Interconnect
- System Interconnect
- Package Interconnect

FFE

Eye @ Slicer

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Accurate Modeling for 16 Gbps or Higher Speeds

- SerDes transmitter and receiver modules
  - Transmitter
    - FFE
    - Edge-boost
    - TX matching network
  - Receiver
    - Rx matching network
    - Continuous-time linear equalizer (CTLE)
    - Variable gain amplifier (VGA)
    - Decision feedback equalizer (DFE)
    - Clock and data recovery (CDR)
Accurate Modeling for 16 Gbps or Higher Speeds

- **Tx AMI**
  - FFE is modelled as C code
  - Boost circuit characterized by step response
  - Tx matching network characterized by step response

- **RX AMI**
  - Tx matching network characterized by step response
  - CTLE, VGA are characterized by step responses
  - DFE, CDR are modelled as C code
  - Data path and a parallel clock path
- Use s-parameters to model matching network in analog portion
  - Boost circuit is implemented at Tx side to improve rise/fall time of the signal
  - Boost circuit is a current-mode driver present in parallel with the voltage mode driver module

Fig5: Tx Edge-boost circuit in parallel path
Accurate Modeling for 16 Gbps or Higher Speeds

- Modeling Boost effects as IR or s-parameters
  - Input signal is differentiated and fed to a voltage-controlled current source. Rise/fall time is improved by pumping extra current at the Tx output node.
  - Assuming boost circuit is linear, enable boost and characterize Tx while terminating in reference impedance. (Repeat steps 1 and 2)
Accurate Modeling of PCIe SERDES IO Using AMI Blocks

- High level of architectural abstraction
- Extremely powerful and flexible
- Capability to model Tx/Rx end to end
- Parameterized blocks
CTE and DFE for PCIe 3.0

\[ y_k = x_k - d_1 \text{sgn}(y_{k-1}) \]
\[ y^*_k = \text{DFE summer differential output voltage.} \]
\[ |y^*_k| = 1 \]
\[ x_k = \text{DFE differential input voltage} \]
\[ d_1 = \text{feedback coefficient} \]
\[ k = \text{sample index in UI} \]
CTE Adapting with DFE
Adaptation can get complex with multiple blocks adapting affecting each other
DFE Only Adaptation at 16Gbps

- CTE Adaptation based on SNR
Adapting CTE May Throw the DFE Off

- CTE Adaptation based on SNR
Changing CTE Adaptation Cycle

- Making the adapt cycle slower may be beneficial
Effects of Changing Adaptation Algorithm for CTE

- CTE adaptation based on 1\textsuperscript{st} DFE Tap
- Digital DFE only updates after 1024 bits instead of every bit (analog).
- Generally takes longer to finish adapting
Parallel Clock Path and Data Path

Clock path

Data path
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What’s in a VRD (Design-in Kit)?

- A **virtual reference design**
  - All the stuff in here:
  - Is modeled here:
  - And simulated/measured here:

Measurement results are replaced with simulation results
What’s in a VRD?

- Parameterized AMI blocks to quickly model various architectures
- Pre-created test-benches to quickly simulate as per compliance
  - Ability to switch channel models
- Ability to quickly transfer PCB/Package model into the test-bench
  - Can estimate Package for given nets and Package size
- Run simulations and get compliance reports
VRD Flow for PCIe 3.0
Choose compliance item

Channel Tolerancing Eye Mask Values (table 4-27 in PCI Express Base spec.)

1. Eye Height
2. Eye Width at Zero Crossing
3. Peak EH Offset from UI Center
4. Range for DFE \( d_i \) Coefficient
5. Eye Mask

Differential Insertion Loss (figure 4-66 in PCI Express Base spec.)

6. Insertion Loss

Differential Return Loss (figure 4-56 in PCI Express Base spec.)

7. Tx Return Loss
8. Rx Return Loss

Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)

9. Stressed/Swept Jitter

Channel Tolerancing Eye Mask Values

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Simulation Results</th>
<th>Pass/Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>25 mV</td>
<td>( V_{RX-CH-EH} )</td>
<td>100.821</td>
</tr>
<tr>
<td>Eye Width at Zero Crossing</td>
<td>0.3 UI</td>
<td>( T_{RX-CH-EW} )</td>
<td>0.425</td>
</tr>
<tr>
<td>Peak EH Offset from UI Center</td>
<td>±0.1 UI</td>
<td>( T_{RX-DS-OFFSET} )</td>
<td>-0.031</td>
</tr>
<tr>
<td>Range for DFE ( d_i ) Coefficient</td>
<td>±30 mV</td>
<td>( V_{RX-DFE-COEFF} )</td>
<td>Pass</td>
</tr>
<tr>
<td>Eye Mask</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Differential Insertion Loss

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Simulation Results</th>
<th>Pass/Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakout Channel Only</td>
<td>SDD21 - Breakout</td>
<td></td>
<td>Fail</td>
</tr>
<tr>
<td>Breakout + Short Calibration Channel</td>
<td>SDD21 - Short</td>
<td></td>
<td>Fail</td>
</tr>
<tr>
<td>Breakout + Long Calibration Channel</td>
<td>SDD21 - Long</td>
<td></td>
<td>Pass</td>
</tr>
</tbody>
</table>

Differential Return Loss

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Simulation Results</th>
<th>Pass/Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx Return Loss</td>
<td>RL - Tx</td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>Rx Return Loss</td>
<td>RL - Rx</td>
<td></td>
<td>Pass</td>
</tr>
</tbody>
</table>
Correlation Techniques

- Three level of correlations
  - Block by block correlations against transistor level simulations
  - Adaption tests against behavioral simulations
  - Tx to Rx link simulations and correlations against Hardware lab measurements
Correlation Results - 1

- Design
  - 16Gbps serial link-PCIe 4.0
  - 16 FinFET technology node
Correlation Results - 1

Testing Analog portion - Step response at TP

Red-Using S-params
Blue-Design simulation
Correlation Results - 2

- Testing pre-emphasis and boost

![Diagram](image.png)
Correlation Results - 3

- Modelling non-linear VGA

**Design Simulation**
- Eye Amplitude: 392mV
- Eye Height: 117mV
- Jitterpp: 0.35UI
- 800 bits

**Model simulation**
- Eye Amplitude: 409mV
- Eye Height: 115mV
- Jitterpp: 0.37UI
- 100,000 bits
Correlation Results - 4

- VGA adaptation
  - VGA codes 0 to 16 for different VGA settings
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  - Our methodology
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Conclusions

- Need parameterized AMI blocks
  - To quickly build AMI models to mimic hardware
  - Allow electrical engineer designer to create AMI models who knows little programming

- Need a flow that allows rapid building of test-benches to cover various correlations at level of:
  - Transistor level simulations
  - Architecture level simulations
  - Hardware lab measurements
References

- http://www.eda.org/ibis/

Acknowledgements

- Taranjit Kukal
- Ritabrata Bhattacharya
- Steve Williams
- Eric Naviasky
- Ken Willis
- Kumar Keshavan
- Ambrish Varma
- Jasleen Ahuja
Thank you for attending the PCI-SIG Developers Conference 2015.

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