

# Voltus-XFi Custom Power Integrity Solution

The next-generation EM-IR solution, delivering over 3X productivity gain

Designers are actively involved in making a greener world for the future by pushing the boundaries of “low-power” enablement. Cadence is providing fast and accurate power analysis tools to enable new and revolutionary ideas on power reduction. The Cadence® Voltus™-XFi Custom Power Integrity Solution is a transistor-level electromigration and IR drop (EM-IR) tool that delivers foundry-supported SPICE-level accuracy for power integrity signoff.

## Overview

Transistor-level EM-IR analysis presents unique challenges ranging from complex EM rules to the high cost of simulating large post-layout RC networks. Integrated with Cadence’s Quantus™ Extraction Solution, Spectre® X Simulator and Virtuoso® ADE Product Suite and Virtuoso Layout Suite, the Voltus-XFi solution delivers the productivity needed to reach aggressive time-to-market goals.

## Benefits

### Accurate and comprehensive analysis

- ▶ Widely supported in foundry process design kits (PDKs) on FinFET and FD-SOI nodes
- ▶ Native support for industry-standard syntax, netlists, abstractions, behavior, and device models
- ▶ Tightly integrated with Spectre simulators to ensure accurate analysis
- ▶ Transistor-level power grid and signal net EM-IR analysis, including accurate resistance network analysis, effective resistance, and least resistance path analysis
- ▶ Support for advanced FinFET analysis features such as self-heating effect (SHE) and failure-in-time (FIT) calculations

### Improved designer productivity

- ▶ Seamlessly integrated EM-IR flow enables designers to complete analysis and debugging easily and quickly
- ▶ Integrated with Voltus IC Power Integrity Solution for advanced custom designs that have mixed transistor-level and cell-level blocks

### Optimized performance for large designs

- ▶ Patented method provides accuracy and capacity with an easy-to-use model
- ▶ Distributed processing optimizes performance by distributing solving nets across multiple cores and machines with load balancing
- ▶ Persistent database for EM-IR results display is optimized for loading and viewing results in Virtuoso Layout, averaging 20X improvement in performance and 2X memory reduction over the existing solution

## Integrated with Cadence ecosystem for fastest design closure

- ▶ Unified electrical signoff flow with Cadence’s Tempus™ Timing Signoff Solution and Quantus Extraction
- ▶ Bring power grid design to the early stage of physical implementation with an early rail analysis capability via the Cadence Innovus™ Implementation System
- ▶ Accurate IC power integrity analysis, driven by real-world power simulation vectors, with Cadence Palladium® technology
- ▶ Benefit from chip-package-PCB co-simulation and analysis with Cadence Allegro® and Sigrity® technologies

## Features

### A central cockpit for EM-IR flow

An EM-IR flow involves many different products, including extraction, design environment, circuit simulation, debugging, and layout viewing. Traditionally, designers must set up each tool and track/handle each product interaction individually, and there is no single place to check EM-IR flow consistency across all the tools. The Voltus-XFi solution solves these problems with a central EM-IR cockpit. It provides a unified setup for the flow by automatically deploying foundry-supported settings. Using the central cockpit, designers can set up and run Quantus extraction, perform EM-IR analysis on a generated or existing DSPF netlist using the Spectre simulator, and invoke and analyze results in Virtuoso Layout Suite (Figure 1).

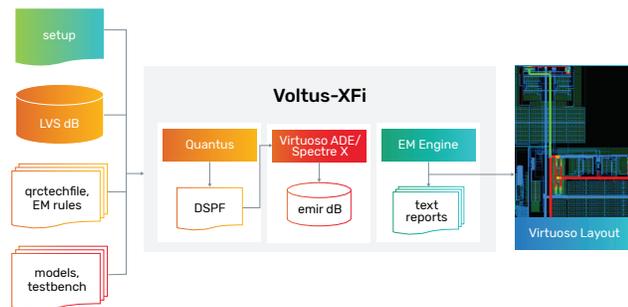


Figure 1: Voltus-XFi solution enables a seamlessly integrated EM-IR flow

### Best-in-class use model with minimum tuning

The Spectre X and Voltus-XFi integration supports the accuracy, performance, and capacity that today’s advanced-node designs require. Like Spectre X, the Voltus-XFi solution balances an accuracy and performance tradeoff for custom IC, mixed-signal, and analog designs with a preset option. In addition, an enhanced method is used to provide a robust and accurate solution: the Spectre solver is used in the first stage, while the second stage uses a specialized RC network

solver with Cadence-patented technology. The method can support larger designs and better performance than the direct method while maintaining Spectre trusted accuracy. For example, complex power-gated networks can be accurately modeled with power-gates switching during the analysis, unlike traditional approaches that model power-gates using as a constant on/off resistance.

### Comprehensive debugging options

The Voltus-XFi solution has a built-in option to ensure that input data are EM-IR ready. An integrated EM-IR results browser (Figure 2) summarizes the EM-IR information and highlights violations, along with details on resistance value, metal layer, width, and length information. The EM-IR results are directly annotated in Virtuoso Layout and make it easy to identify and fix the problem area.

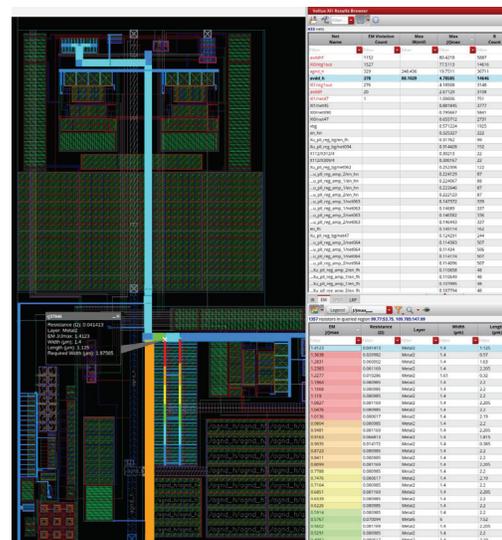


Figure 2: Voltus-XFi EM-IR results browser

### Full chip support with Voltus integration

The Voltus-XFi solution can generate a power-grid-view (PGV) macro model for the transistor block/IP being analyzed and pass this to the Voltus IC power integrity solution for full-chip signoff. A PGV macro model is a binary model that describes an IP’s grid characteristics. It contains geometric views, port information, current information, and multi-mode multi-corner (MMMC) features in capturing various operational modes, voltages, and clock frequencies. The Voltus-XFi solution generates the most accurate views, and the Voltus IC power integrity solution applies the correct view for full-chip signoff.

## Supported Formats

- ▶ DSPF netlist (Quantus and third-party extractors are supported)
- ▶ Spectre and SPICE netlist formats
- ▶ Spectre, SPICE, and PSpice® models
- ▶ Verilog-A 2.0 LRM-compliant behavioral models and structural netlists
- ▶ S-parameter data files in Touchstone, CITI-file, and Spectre formats
- ▶ SST2, PSF, PSF XL, and FSDB waveform formats
- ▶ Digital vector (VEC) and Verilog-Value Change Dump (VCD)
- ▶ Extended Verilog-Value Change Dump (EVCD) and digital stimulus

## Platform Support

- ▶ Build OS: RHEL 7.4
- ▶ Supported OS: RHEL 8, RHEL 7 (>=RHEL 7.4), SLES 12

## Cadence Services and Support

- ▶ Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- ▶ Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- ▶ More than 30 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- ▶ Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, Rapid Adoption Kits, software downloads, and more.
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