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Tempus Timing Signoff Solution

Distributed STA with integrated layout fixing

The Cadence® Tempus™ Timing Signoff Solution is the fastest static timing analysis (STA) tool in the industry today with unique distributed processing and cloud capabilities enabling hundreds of CPUs to quickly complete even the largest designs. With full foundry certification and a comprehensive set of advanced capabilities, the Tempus solution delivers SPICE-accurate results to hundreds of customers across a broad range of design types: from the largest 5nm designs, to high-volume mobile designs, and mixed-signal chips on mature processes.

Overview

The Tempus solution is a modern tool designed to tackle the most advanced timing requirements including full signal integrity (SI) analysis, statistical variation (SOCV), multi-mode and multi-corner analysis, static and dynamic power, and glitch.

More than just an analysis tool, the Tempus solution is also deeply integrated with Cadence's Innovus™ Implementation System, Quantus™ Extraction Solution, and Voltus™ IC Power Solution. By tightly coupling design implementation with timing signoff, the Tempus solution speeds timing convergence throughout the design flow and greatly reduces the time to design closure.

Key Features and Benefits

- Industry's fastest runtimes with advanced distributed STA to over 100 CPUs and the cloud
- Integrated with Innovus Implementation System for faster timing closure with physically aware signoff timing engineering change orders (ECOs)

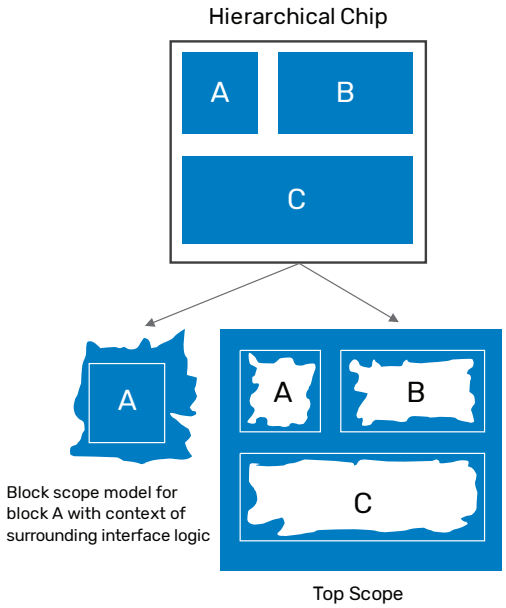

Figure 1: SmartScope hierarchical models allow physical ECO optimization of paths crossing hierarchical boundaries

- Integrated with Voltus IC Power Solution for timing-aware IR-drop fixing
- Fully certified down to 3nm
- Concurrent multi-mode and multi-corner (CMMMC) technology delivers 5X faster runtime without any loss in accuracy
- Support for accurate statistical on-chip variation (SOCV) analysis and ultra-low voltage effects
- Automatic parasitic extraction with the Quantus Extraction Solution
- SmartScope™ hierarchical abstraction models provide the same accuracy as flat STA in a fraction of the runtime and support full in-context timing ECOs
- Integrated with Cadence Virtuoso® full-custom design platform with cross-probing of timing paths between the timing report and layout

Distributed Processing and Multi-Threading

Every Tempus timing job is naturally multi-threaded for faster execution on 16 CPUs and more. But the Tempus solution also has the unique capability to distribute an STA job across multiple separate machines that each take advantage of multi-threading in their own memory space. This delivers significantly faster runtimes and reduces the memory requirements for each machine. Distributed STA is essential to analyze today's extremely large designs in acceptable time and for execution in the cloud.

Concurrent Multi-Mode Multi-Corner

The Tempus solution can automatically distribute STA jobs for each mode/corner combination (or "view") across multiple machines where each machine times the full design for a single view. In the end, all the results are collected into a consolidated report.

Even more powerful is the Tempus solution's unique concurrent multi-mode multi-corner (CMMMC) capability, which processes multiple views concurrently in a single STA job. CMMMC exploits the commonalities between views to deliver a 5X faster runtime without any loss in accuracy and with a full, detailed timing report for each view. This technology is a critical accelerator when analyzing designs across many mode/corner combinations.

Signal Integrity

Every Tempus license includes a complete SI analysis engine that calculates all relevant timing windows and their overlaps to correctly model crosstalk effects on timing.

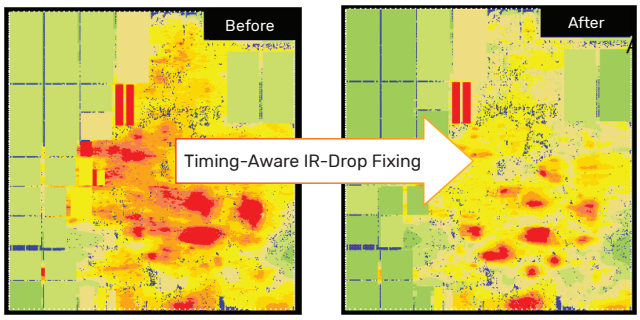

Figure 2: The Tempus ECO Option is integrated with Innovus physical implementation and Voltus voltage drop analysis for signoff accurate timing and power optimization

Power Analysis

The Tempus solution will report the dynamic (switching) and static (non-switching) power used by a circuit. This calculation can be made based on user-supplied activity files or through vectorless activity profiles.

Statistical OCV

The Tempus solution offers statistical OCV to reduce unwarranted pessimism caused by on-chip variation. The Tempus solution supports both the Cadence SOCV library format and the Liberty Variation Format (LVF) for statistical library characterization. The Tempus solution can also accurately model and calculate the ultra-low voltage effects at 7nm and below that cause the statistical variation to be non-symmetrically skewed about the mean (third moment).

Hierarchical Models and SmartScope

The Tempus solution has dramatically improved runtime and capacity so almost all design sizes can now be analyzed flat. However, it is common for subsets of the design to go through final iterations before tapeout and the Tempus solution offers a range of hierarchical modeling options including traditional static models like extracted timing model (ETM) and interface logic model (ILM). But to facilitate signoff-accurate ECOs, the Tempus solution offers SmartScope models for block and top-level. Scope models dynamically abstract only those portions of the design that a user wants to analyze and do it in a full chip-level context, including SI and all physical effects.

Tempus ECO Option with Innovus Implementation

The Tempus solution is integrated with the Innovus Implementation System where it drives signoff-accurate and physically aware timing ECOs that significantly shorten time to market, reduce power consumption, and eliminate wasteful timing margin.

The Tempus ECO Option fixes setup, hold, glitch, and design rule violations. It can also optimize the design for dynamic power, static power, or total power.

For more than just logical changes, the Tempus ECO Option is physically aware and can see physical congestion and understand all placement rules so that cells are always legally placed. It is also routing aware so that buffers are inserted directly on an existing route for optimal timing convergence.

Timing-Aware IR Drop with Voltus Power

The close integration between the Tempus, Innovus, and Voltus solutions allows voltage drop analysis, and IR drop issues to be automatically fixed by downsizing aggressors that cause IR drop on critical paths, while preserving timing. The same integration also makes it possible to analyze clock jitter with IR drop and activity effects included.

Integration with Virtuoso Platform

The Tempus solution is available within Cadence's Virtuoso custom design platform through seamless data integration with its Open Access database. The Tempus solution is available as part of the Virtuoso Digital Signoff package for small embedded digital logic in mixed-signal designs. It includes cross-probing of timing paths between a timing report and the Virtuoso layout editor, automatic abstraction of digital components, parasitic extraction, and SDC integration.

Common User Interface

A new common user interface is shared with the Innovus, Voltus, and Tempus solutions to streamline flow development and simplify user trainings across a complete Cadence digital full flow.

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (ILS) online courses allow you the flexibility of training at your own computer over the Internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more.
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