

Stratus High-Level Synthesis

Fastest path from specification to silicon

Cadence® Stratus™ High-Level Synthesis (HLS) automatically creates high-quality register transfer level (RTL) design implementations for ASIC, system-on-chip (SoC), and FPGA targets from high-level IEEE 1666 SystemC™, C++, and MATLAB® descriptions. The proven successes of Stratus HLS in production designs around the world are testament to its consistently high-quality results, mature feature set, and complete design coverage. While most widely used for image processing, wireless, and machine learning (ML) applications, products built with Stratus HLS technology can be found in your home, automobile, and pockets.

Overview

With Stratus HLS, engineering teams can quickly design and verify high-quality RTL implementations from abstract IEEE 1666 synthesizable SystemC, C, C++, or MATLAB models. The models can be easily created using the Stratus integrated design environment (IDE). Stratus synthesizable SystemC IP provides simulation and synthesis models for common bus-based and point-to-point communication protocols as well as common mathematical operations and datatypes.

Leveraging Cadence's Genus™ synthesis and Joules™ power engines inside of Stratus HLS, the power, performance, and area (PPA) results are typically equal to or better than those achieved with hand-written RTL. Front-end designers get high-quality PPA estimates through turnkey integration with the Cadence digital flow.

With Stratus HLS, SystemC models can be retargeted to new technology platforms and reused more easily than traditional hand-coded RTL. The Stratus graphical user interface (GUI) also allows designers to actively and quantitatively evaluate PPA tradeoffs from within the high-level synthesis environment.

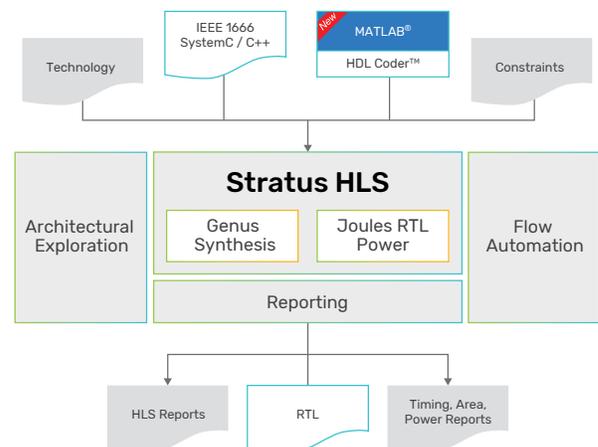


Figure 1: Stratus HLS uses the Genus synthesis and Joules power engines to create high-quality RTL targeted to your technology and design constraints

Stratus HLS automates the design and verification flow of hundreds of blocks from transaction-level models (TLMs) to gates. In addition, Stratus HLS helps with the real-world issues of engineering change orders (ECOs) and routability, both of which normally occur much later in the flow, through tight integration with the full Cadence tool flow.

Key Benefits

- ▶ Supports industry-standard IEEE 1666 SystemC, C, and C++
- ▶ Integration from MATLAB to Stratus HLS gives algorithm developers early and accurate visibility to PPA and gives RTL authors an automated path from MATLAB to optimized RTL, yielding an optimized micro-architecture and eliminating manual translation from MATLAB code to RTL
- ▶ Industry-leading quality of results (QoR) through advanced sixth-generation HLS optimizations and tight integration with the Cadence digital implementation flow
- ▶ Genus synthesis engine inside of Stratus HLS improves QoR by creating the exact custom datapath components needed for the design
- ▶ Genus logic synthesis and Joules power engines inside of Stratus HLS provide accurate timing, area, and power estimates
- ▶ Predictable downstream closure through turnkey integration with Cadence digital full flow
- ▶ Wide applicability across the full design space, including both control-centric and datapath-centric designs
- ▶ Support for hierarchical design and verification, including multiple modules and threads
- ▶ IEEE 1666 SystemC simulation and synthesis models for common bus-based and point-to-point I/Os, fixed-point and floating-point operations of user-defined precision, and common math and library functions
- ▶ Advanced pipelining optimizations support fully pipelined and partially pipelined designs with stalling, draining, and bubble squashing
- ▶ Top-down and bottom-up support for ECOs
- ▶ Up to 50% power reduction through low-power optimizations
- ▶ Reduction of routing congestion via physically aware high-level synthesis
- ▶ Automated support for multiple synthesis scenarios enables quantitative design space exploration and optimization
- ▶ Synthesis of SystemC assertions and C++ asserts to SystemVerilog assertions (SVAs)

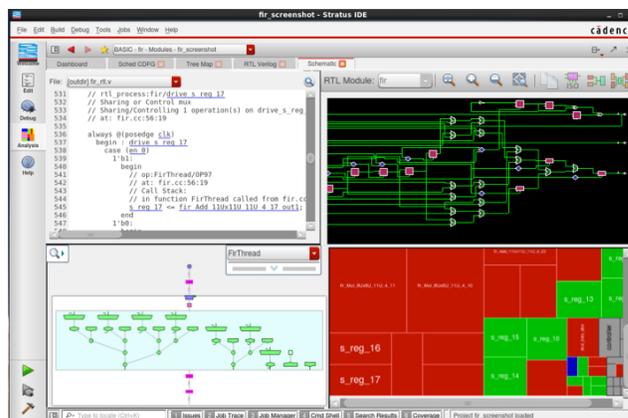


Figure 2: Complete graphical analysis with links to source code

- ▶ Automated design and verification of hundreds of blocks with a consistent verification environment from TLM models through gates, including mixed-language (SystemC and RTL) simulation and debug
- ▶ Equivalence checks between RTL scenarios with Cadence Jasper™ formal verification integration
- ▶ Stratus HLS knowledge base (<http://support.cadence.com/StratusHLS>) online support with getting started guides, design examples, best practices, and application notes

Features

IEEE 1666 SystemC, C, C++ Synthesis

Stratus HLS supports industry-standard IEEE 1666 SystemC as well as C and C++ semantics.

The SystemC class library provides modularity, concurrency, and bit-accuracy, allowing designers to use familiar hierarchical decomposition techniques to manage design complexity. By supporting hierarchy and multiple threads, SystemC allows design and verification of algorithms and their interfaces operating concurrently.

Stratus HLS also allows C or C++ algorithmic code to be automatically put into the context of a hardware module with hardware interfaces.

Broad Applicability

Silicon built with Stratus HLS is in billions of products worldwide. While most widely used for image processing, wireless, and ML applications, products built with Stratus HLS can be found in a wide range of silicon applications.

Stratus HLS supports untimed and timed SystemC and C++ models, including a mix of both, providing maximum flexibility to the designer. The output can be fully pipelined (new data each cycle), pipelined at reduced throughput (new

Design and Verification Flow Automation

Stratus HLS comes with a fully integrated automation system. One short Tcl file can configure and automate all of the following.

- ▶ C++ compilation and linking
- ▶ Synthesis directives
- ▶ SystemC and RTL simulation
- ▶ Analysis and debugging of SystemC, RTL, or a combination of both
- ▶ Waveform analysis
- ▶ Synthesis of assertions
- ▶ Formal equivalence between multiple RTL implementations
- ▶ Logic synthesis
- ▶ Power analysis
- ▶ Results visualization
- ▶ Design exploration for multiple configurations
- ▶ Quantitative tradeoff analysis

This automation allows designers to use Stratus HLS to explore multiple architectures and implementations while improving verification by providing a consistent environment from early TLM models through gates.

ECO Support

Changes to the design can become necessary at any point during the design flow. When those changes come late, the ECO mode of Stratus HLS can enable you to still meet your deadlines.

Rather than creating new RTL and completely redoing the entire RTL-GDSII implementation, Stratus HLS creates an RTL implementation with minimal changes so that Cadence Conformal® ECO Designer can create an ECO patch to minimize the impact of the change on the design and thus the schedule.

Working in conjunction with Conformal ECO Designer, the patch can be applied on the netlist, the placed design, the routed design, or even the post-mask netlist if a metal-only ECO is possible. This ensures the patch is correct and that the design still meets its quality of results goals.

Low-Power Optimization

With Stratus HLS, design teams can automate complex low-power optimizations that are often difficult or impossible to realize with hand-coded RTL, such as fine-grained and block level clock gating, FSM optimizations, and power-aware scheduling (re-ordering) of operations.

Designers can use the exploration capabilities of Stratus HLS to quickly trade off design PPA. For some applications, additional criteria may be included in the tradeoff analysis, such as ML accuracy or implementation loss for wireless applications.

These optimizations can yield power reductions of 50% or more, depending on the design.

Design Closure

Stratus HLS ensures easy timing closure for the generated RTL by exhaustively analyzing each path and scheduling operation so they fit in the given clock period.

Stratus HLS uses patented datapath optimization technology and the embedded Genus synthesis to build all datapath components, multiplexers, and registers in the specified technology library to get accurate timing and area models.

The user can control how aggressively Stratus HLS packs these operations into each clock period. Creating designs with Stratus HLS can save months of back-end effort by preventing timing closure problems.

Integration with Genus physical synthesis allows early visibility and feedback into likely congestion problems, allowing the front-end designer to avoid problems in the back-end.

Behavioral IP Reuse

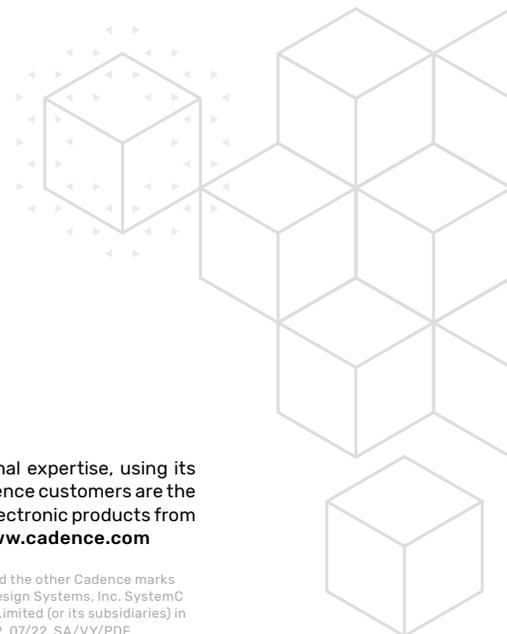
Stratus HLS enables the creation and adaptation of behavioral IP, delivering on the promise of true IP reuse.

Using Stratus HLS, the verified source code can be reused without modification for widely different process technologies, clock speeds, or PPA targets. Modifications to the algorithm, architecture, or interfaces can be made incrementally at a high level, where previously they required a complete RTL rewrite.

Behavioral IP reuse with Stratus HLS significantly reduces overall design effort and maximizes return on investment (ROI).

Cadence Services and Support

- ▶ Cadence application engineers can answer your technical questions by telephone, email, or internet—they can also provide technical assistance and custom training.
- ▶ Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- ▶ More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- ▶ Cadence Online Support gives you 24x7 online access to a knowledge base of the latest solutions, technical documentation, software downloads, and more.
- ▶ For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.



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