Quantus Smart View—Next-Generation Extracted View

Cadence® Quantus® Smart View is the next generation of the current market-leading Extracted View, a flow that Cadence pioneered over a decade ago for faster circuit debugging and post-layout verification and simulation.

Introduction

Extracted View and the Extracted View flow is widely used by designers today for circuit debugging and for post-layout verification and simulation. It is a graphical representation of the parasitic netlist that allows tight integration into the Cadence Virtuoso® Environment. Extracted View provides unique capabilities, such as parasitic cross-probing to devices of interest, allowing designers to query nets, identify shapes contributing to high parasitics, and take corrective action by changing the layout. Furthermore, it enables back-annotation of lumped parasitic values into the schematic for easy visualization. During simulation, designers can substitute Extracted View instead of schematics for accurate post-layout analog simulation.

In addition, Extracted View is a critical part of the EM and IR analysis with the Cadence Voltus™-Fi Custom Power Integrity Solution. Designers can use Extracted View to get a visual representation of the hotspots for further analysis.

Increase in Design Complexity and Sizes

The post-layout simulation flow is very important for any custom/analog design because it allows a designer to verify, debug, and ensure the design specifications are met (i.e., verify what you designed will in fact be exactly what you will see in silicon) before final tapeout. However, with the complexity of the designs increasing, especially at advanced and FinFET nodes, the designs are getting bigger with an increase in the number of devices exponentially increasing the total number of parasitics. This creates a netlist that is bloated and significantly impacts extraction runtimes, netlist size, and the Virtuoso ADE Product Suite’s ability to create a netlist in a reasonable time for simulation. The current Extracted View can be taxed trying to handle the larger, more complex designs and advanced nodes.
Innovation to Help Our Customers

Quantus Smart View is based on a completely new architecture that utilizes massively parallel technology to significantly improve the performance. It addresses the performance and capacity issues for all designs and for all technology nodes.

**Total Extraction Runtime**

\[ f \text{ (Input, LVS DB + Quantus Extraction Runtime + Smart View Generation Runtime)} \]

The new architecture enables a faster generation runtime, which reduces overall extraction runtime, and a reduction in netlist size, resulting in the Virtuoso ADE platform’s ability to netlist faster than its predecessor. Additionally, the Quantus Smart View output is based on the DSPF format instead of SPICE, thereby enabling direct support for FastSPICE tools such as Cadence Spectre® eXtensive Partitioning Simulator (XPS).

Benefits and Attributes of Quantus Smart View

- Delivers the fastest path to post-layout verification and simulation with up to 10X performance improvement
  - Up to 7X faster than Extracted View
  - Up to 7X smaller netlist size than Extracted View
  - 10X faster Virtuoso ADE netlisting turnaround time
- Same usability and integration within the Virtuoso platform
  - Provides key post-layout simulation verification functionality, such as in-context cross-probing, back annotation, and single Smart View for multiple process corners
- DSPF file format output allows direct support for FastSPICE tools such as Spectre XPS
- Enables faster verification and simulation runtimes with Spectre Accelerated Parallel Simulator (APS) and Spectre XPS
- No additional foundry enablement is required to support files such as .trp or icellmap

![Fig 3: Voltage waveforms (in-context) probing](image-url)