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How to Speed Signoff Extraction by 5X with Next-Generation Extraction Tool

Tool Contributes to Faster Overall Design Closure

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Parasitic extraction, particularly in the digital world, is becoming an increasingly time-consuming process. Not surprising, considering the explosion in interconnect corners, increasing design sizes and number of parasitics, and complex modeling features at advanced nodes, including FinFETs. This paper discusses capabilities you should have in order to overcome parasitic extraction challenges, and introduces our next-generation extraction tool built on a proprietary massively parallel architecture that speeds signoff extraction turnaround time (TAT) up to 5X and provides best-in-class accuracy, as well as custom analog flows.

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Introduction

Parasitic extraction is an important means to an end, since it enables you to provide accurate data on parasitic effects in resistances, capacitances, and other areas of interconnect wiring for the timing analysis and post-layout simulation steps. Complex analog/mixed-signal (AMS) systems on chip (SoCs) are particularly prone to design closure challenges, as the analog circuits are extra sensitive to noise and the effects of parasitic resistance and capacitance. Being able to assess the impact of parasitics during schematic simulation fosters better design convergence.

As a final step before tapeout, extraction can evoke both joy ("Yay, we're ready to start making masks and wafers!") and anxiety ("Ah, did we resolve all of the parasitics in our design?"). However, at advanced nodes, especially for FinFET designs, there are greater challenges to successful signoff extraction. Having an accurate way to overcome these challenges is critical. Perhaps even more urgent—given today's time-to-market pressures—is the need to accelerate signoff extraction TAT. Traditional rules-based extraction tools are no longer accurate enough to validate electrical performance in advanced-node designs. In fact, until now, the market has lacked tools that deliver the performance required to produce a significant speed-up in this flow. In this paper, we'll examine key capabilities in a next-generation parasitic extraction tool that will equip you to reduce total extraction time from about six weeks down to about three weeks or less.

Why Has Signoff Extraction Become So Challenging?

At advanced nodes, signoff extraction has become quite challenging due to a number of reasons:

- There's been a rise in the number of interconnect corners on both the digital and custom/analog sides. At 20nm and below, there are 3X more corners for double-patterning technology (DPT). To ensure that there's no variation in your process corners, you have to perform stress tests to assess response times at different temperatures—a laborious and time-consuming process.
- Design sizes are increasing. At 20nm and below, there are more than 70 million net designs. With more corners and larger design sizes, extraction goes from taking a day to a few days to complete.
- The number of parasitics is increasing. There are 155X more resistances for FinFET than 28nm devices, for example. In FinFET designs, the growth in parasitics is resulting in bigger netlists, which impacts post-layout simulation performance and requires faster simulation runtime.
- From FinFET to fringe capacitances, DPT, and more, modeling features have grown more complex, increasing the extraction runtime
- Often, different extraction engines are used in implementation and signoff, resulting in poorly correlated results that have a negative impact on design closure

To overcome the main challenges of signoff extraction at advanced nodes, look for an extraction tool with these three key capabilities:

- In-design integration for both digital and custom/analog platforms. When such integration is in place, there is better correlation and support for faster design convergence. This is particularly critical for FinFET designs, where you will want to maintain some control over parasitics correlation in implementation and signoff, or else risk spending an enormous amount of time fixing issues and delaying tapeout.
- Field solver and extraction engines with better accuracy algorithms
- Scalability across multiple CPUs and machines

Next-Generation Extraction Tool with 5X Better Performance

Cadence has introduced a next-generation extraction tool for custom analog and digital flows that provides at least 5X better performance than competitive products on the market. In one benchmark involving 16 CPUs and Gds input data, Quantus™ QRC Extraction Solution demonstrated 6.2X faster total runtime of TOP level, compared to competitive products. In another benchmark, under the same conditions, the Cadence® solution achieved 7.6X faster total runtime against the competitors.

Cadence Quantus QRC Extraction Solution features massively parallel technology, delivering high performance across multiple CPUs; the tool scales easily beyond 128 CPUs. Built with the same high-accuracy modeling engines as its predecessor, Cadence QRC Extraction, Quantus QRC Extraction Solution uses the same foundry-qualified, unified "qrctechfiles" for digital and transistor extraction, including substrate noise analysis for all nodes. In addition, the tool is fully certified for the 16nm FinFET process at TSMC.

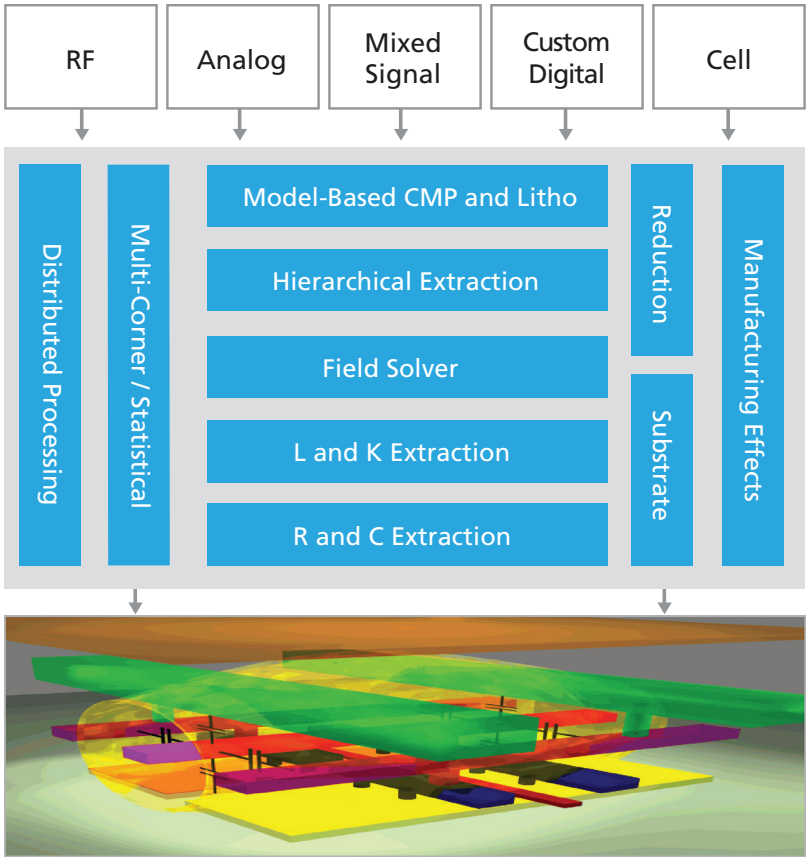

Figure 1: Primary capabilities of Quantus QRC Extraction Solution

Let's take a closer look at the key capabilities of the Quantus QRC Extraction Solution.

Accuracy

When a design has tens of millions of nets, running field solver for parasitic extraction is much too time-consuming. Designers of large designs will generally run a field solver on selected random nets to collect some data, then run an extraction tool to correlate the data and determine the differences.

Quantus QRC Extraction Solution delivers tighter accuracy against stand-alone field solvers with a near-zero mean. The tool's embedded field solver technology, called Quantus FS, equips it to deliver accurate critical nets extraction. In a recent customer benchmark on a 20nm design, the tool achieved a mean of -0.01 (the standard deviation was 3.09), compared to field solver on 1,000 random nets.

Scalability and Performance

With the new extraction tool and its massively parallel technology, you can double the number of CPUs and achieve a nearly 2X performance gain. For example, moving from 16 to 32 CPUs can reduce extraction time from 72 hours down to 36 hours. The tool scales for single- and multi-corner extraction runs; in fact, the tool performs 2X to 3X faster in multi-corner runs. A recent benchmark with four RC corners and two temperatures showed an approximate 3X runtime improvement. A single license supports simultaneous extraction of five process corners, without any compromise on accuracy.

Compared to competitive products, Quantus QRC Extraction Solution has demonstrated better capacity handling and performance for advanced nodes.

Better Signoff Flow Turnaround Time

Since the tool utilizes automated incremental extraction, users experience better TAT at signoff. Automated incremental extraction eliminates the need for full-flat extraction for functional engineering change orders (ECOs) at the block level and at full chip. Quantus QRC Extraction Solution integrates with Cadence Encounter® Digital Implementation Solution. When you make any routing changes, this information is stored in the Encounter Digital Implementation System database; the Encounter solution passes this information over to the extraction tool, eliminating a manual process.

As an example of the faster performance, consider a customer's 20nm design with 210K nets. Running incremental extraction on two CPUs took 2.5 minutes—a 5.5X faster extraction time vs. full-flat extraction, without any accuracy loss for TCap and Ccap.

Incremental extraction has proven to be as accurate as using standalone signoff full-chip extraction (including with metal fill). The tool supports all place-and-route tools.

16nm FinFET Leadership

The FinFET process introduces additional new parameters that call for complex modeling for better accuracy. The explosion in parasitics results in a bigger netlist, which impacts post-layout simulation performance and requires faster turnaround time for digital designs. Among the parasitic challenges in capacitance and resistance at this process:

- Fringe 3D capacitances from gates and fins
- New capacitances components to fins from gate thickness
- External capacitances to M0/V0 (middle end of line [MEOL]) contacts
- Explosions of resistance, requiring better handling techniques to expedite post-layout simulation

The biggest impact is below Metal 1, where the following front end of line (FEOL) features must be considered:

- Multi-finger fins per device with varied pitches and widths
- Complex poly structures
- Raised source drain
- Two-step M0

Additionally, FinFET processes also have BEOL modeling requirements similar to those in double-patterning technology. Examples include litho bias, corner variations, and mask shift variations.

By establishing a deeper integration of signoff extraction in the place-and-route process, designers can achieve better post-route optimization, better turnaround time with incremental extraction, and better convergence to signoff with metal fill estimation. After all, with the FinFET process, designers can no longer afford to wait and see the impact of parasitics at post-layout simulation. Better design convergence comes via early assessment during schematic simulation.

Benchmark tests have revealed that Quantus QRC Extraction Solution, tapping into a robust 3D modeling framework, offers unmatched accuracy vs. the foundry golden. Compared with competitive solutions, the tool provides 2.5X faster netlist simulation runtime, with a 2X smaller netlist and faster characterization of standard cells, SRAMs, and IP.

Better Design Convergence

In a FinFET process, device parasitic resistances and capacitances adversely impact circuit timing—and even more so as devices shrink in size. Studies comparing standard cells at 16nm and at 20nm show 20-67% increases in timing delays with pre-layout simulation and post-layout simulation.

Used with a gate/source capacitance (Cgs) flow based on Cadence Virtuoso® Analog Design Environment, Quantus QRC Extraction Solution contributes to faster design convergence. The engineer would have earlier visibility into parasitics in the schematic. By comparison, in a regular flow, there would be a large gap between intended and expected results, at the pre-layout simulation and post-layout simulation levels.

As discussed previously, Quantus QRC Extraction Solution is also integrated with the Encounter Digital Implementation System. Within Encounter Digital Implementation System, a deterministic solution for physical implementation of complex SoCs, users gain single-click execution for all extraction models. Using the same engine in both tools for place-and-route and for signoff provides better and faster design convergence.

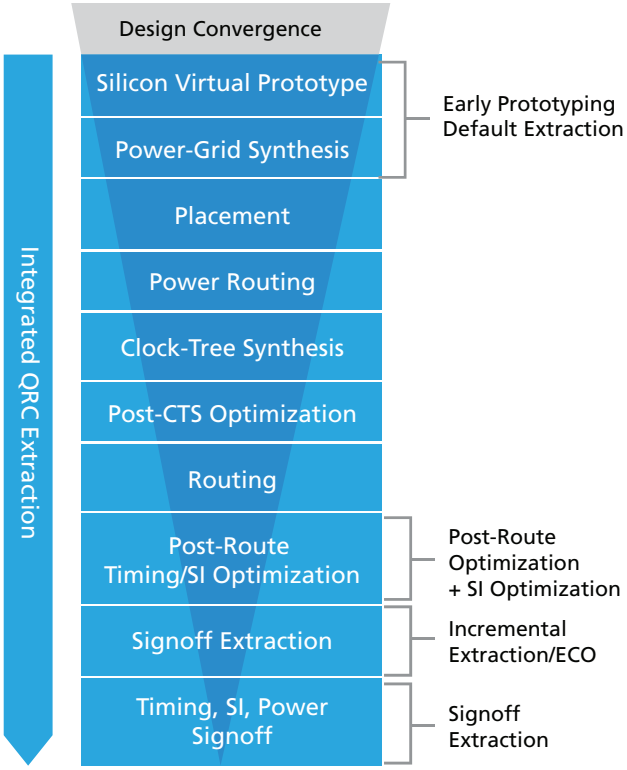

Figure 2: Quantus QRC Extraction Solution integrates with Encounter Digital Implementation System, together fostering better and faster design convergence.

Unique Functionality for All Design Types

Quantus QRC Extraction Solution supports all design types, including:

- Custom/analog and RF designs
- SerDes
- IP/SRAM/bitcell characterization
- Memory, PowerMOS, image sensors

For these design types, the tool provides unique functionality:

- Substrate noise analysis, with a full 3D substrate model and support for full-chip and block levels
- Inductance extraction supporting LEF/DEF flow, which helps analyze parasitic impact, especially for CLK and longer nets
- Inductance extraction, with support for Partial Element Equivalent Circuit (PEEC) method and mutual and self-inductance
- MeshR, providing better accuracy for all irregular or wide metal shapes. Users define the mesh size based on the smallest feature size. The adaptive meshing technique improves simulation runtime by reducing the number of resistances extracted (a smaller netlist size results). Large grids are at the center of the die, covering a large area; fine grids are near contacts, edges, and corners; and coarser grids are away from contacts.
- RCLK reduction, with support for both RC and RCLK reduction at a 20X simulation time reduction

Summary

From mobile and smart connected devices to cloud computing, the opportunities driving semiconductor innovation are huge. These market opportunities present conflicting challenges for design engineers: they are working on SoCs that are much more complex to design while facing pressure to get to market faster than their competitors. Parasitic extraction, especially in the digital world, is one step in the design flow that can be particularly time-consuming, especially at advanced nodes. Having an extraction tool with the right capabilities for complex, advanced-node SoCs—such as Cadence Quantus QRC Extraction Solution—can shorten the signoff extraction step considerably. With high accuracy and scalability, along with in-design integration for digital and custom/analog platforms, Quantus QRC Extraction Solution can accelerate signoff extraction by 5X, contributing to an overall faster design closure process.

For Further Information

To learn more about Quantus QRC Extraction Solution, visit: www.cadence.com/products/di/quantus_qrc_extraction/pages/default.aspx.

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