



Quantus FS—Industry’s First Cloud-Ready, Massively Parallel 3D Extraction Solution

RLCK extraction you trust!

The Cadence® Quantus™ FS (Field Solver) Solution is a built-in 3D capacitance field solver offered with the Quantus Extraction Solution. This random-walk-based field solver can handle any capacity, provides faster turnaround times, and provides best-in-class accuracy.

Introduction

The Quantus FS solution has been certified and qualified at multiple foundries and provides better accuracy versus foundry golden. It supports both LEF/DEF- and GDS-based designs for signoff extraction, and is production proven at multiple customer sites with multiple tapeouts, ensuring on-time tapeout and first-time silicon success.

3D Problems Require 3D Solutions

The Quantus FS solution raises the bar for signoff parasitic extraction turnaround time for all types of designs at all technology nodes. The Quantus FS solution provides a breakthrough in 3D parasitic extraction by introducing cloud- ready and massive parallelism that significantly improves the performance of 3D field solvers, while allowing designers to get the accuracy of a 3D field solver.

Design	Customer Requirement
Standard Cells	<ul style="list-style-type: none"> • 3D signoff accuracy for all types of designs • Characterize 1000s of standard cells (custom cells) with 3D accuracy in minutes • Re-characterize library to verify .lib, .v, and timing/power/noise models • Characterize 1000s of SRAMs with better accuracy to improve the performance of design—especially for high-frequency designs and low-/ultra-low-power designs • Signoff accuracy required for all types and shapes of vias, a memory design for accurate R extraction • Smallest netlist to expedite simulation runtimes
SRAMs	
Other Memory (DRAM, flash, etc.)	
AMS/Interface IP	
Automotive (Sensors)	

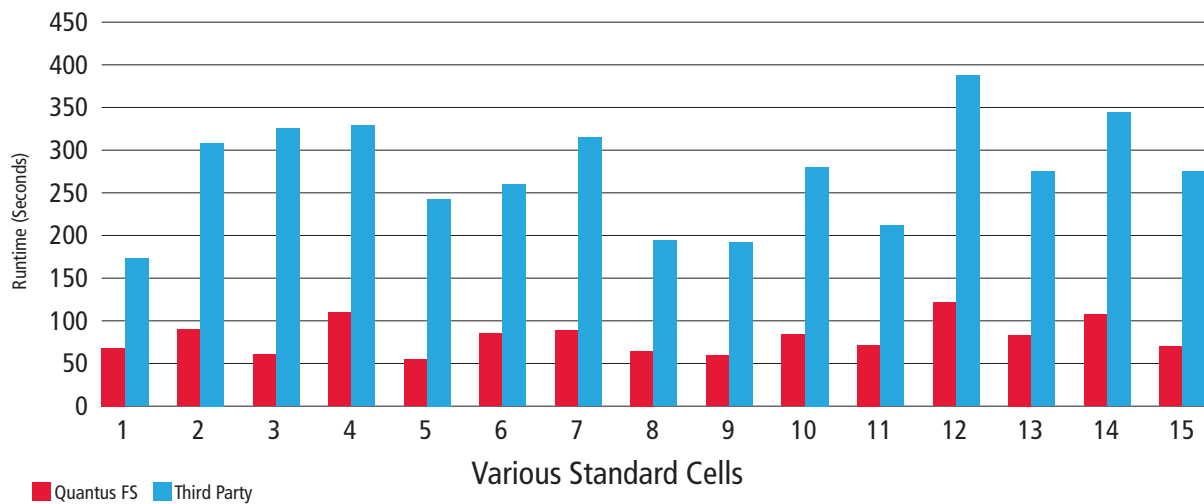


Figure 1: 3X Faster vs Competition—10nm Standard Cells—16CPUs

This new cloud-ready, massively parallel Quantus FS solution addresses the challenges faced for design characterization and other critical design types, which typically require 3D accuracy but can't afford the performance of a 3D field solver. Now designers are empowered to use a field solver solution to get 3D accuracy without compromising performance..

The Quantus FS solution specifically addresses the following design types:

- Standard cell characterization
- SRAM characterization
- AMS and interface IP (PLL, VCOs, PHY, DDRs, other sensitive designs, etc.)
- All other memory designs (DRAM, MRAM, flash, etc.)
- Automotive designs (lidar and other sensors)

Benefits of the Quantus FS solution:

- Cloud ready and massively parallel
 - Linear scalability to 1000s of CPUs
 - Produces smallest netlist
 - Lowest memory consumption
- Foundry certified down to 7nm and for latest versions of 5nm at TSMC
 - Best-in-class accuracy versus foundry golden data
 - Certified at many foundries
- Integrated in Quantus Extraction Solution and other Cadence tools
 - Innovus™ Implementation System, Virtuoso® Custom Design Platform, Voltus™-Fi Custom Power Integrity Solution, and Tempus™ Timing Signoff Solution
 - Virtuoso Liberate™ Characterization Solution
 - Spectre® Accelerated Parallel Simulator (APS) and Spectre eXtensive Partitioning Simulator (XPS)

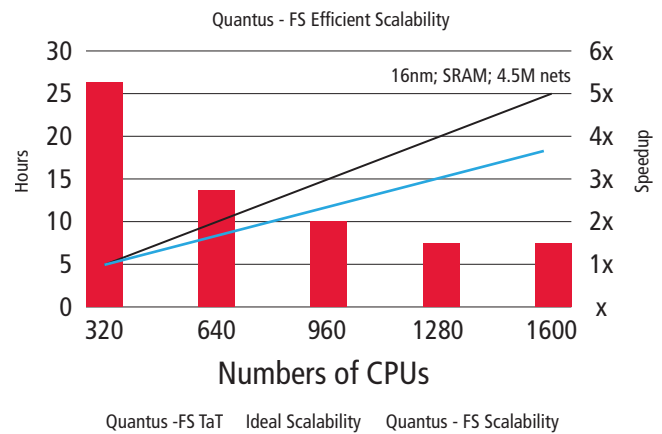


Figure 2: Cloud-Ready Linear Performance—SRAM Design

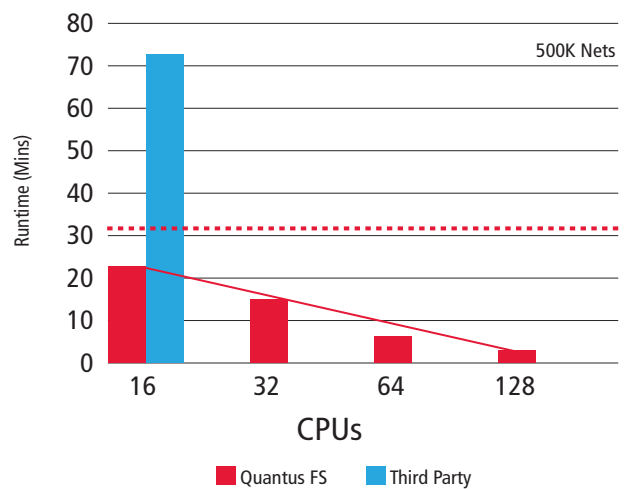


Figure 3: Cloud-Ready Linear Performance—DRAM Design

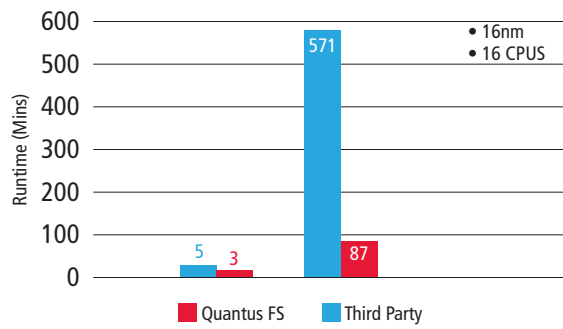


Figure 4: PLL Performance—7X Faster than Competition

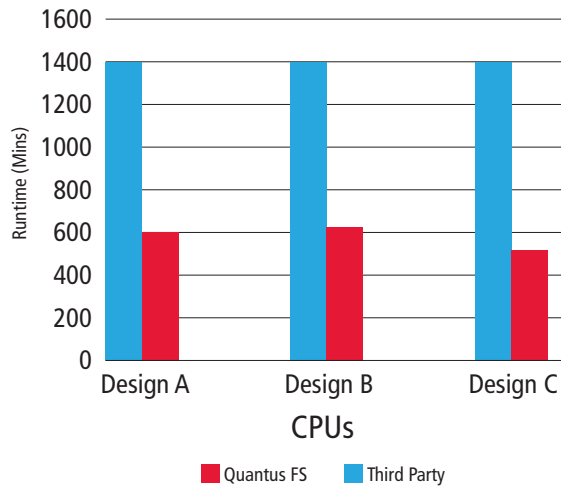


Figure 5: Smallest Netlist—~3X Faster Simulation Runtime vs Competition

Summary

For advanced nodes, specifically FinFET, 3D field solver accuracy is a must. Designers can no longer afford to compromise on accuracy as it may lead to performance loss and convergence issues for SoCs and other designs. The Quantus FS solution removes the bottleneck of performance for a field solver while providing the accuracy required.

Further Information

To learn more about the Quantus FS solution, visit <https://www.cadence.com/go/quantus-extraction>.



Cadence software, hardware and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. The company's System Design Enablement strategy helps customers develop differentiated products—from chips to boards to systems. www.cadence.com

© 2018 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. All other trademarks are the property of their respective owners. 11058 08/18 SA/RA/PDF